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OCTOBER 8, 1984
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ElectronicsWeek®

CMOS chips aid signal processing AS FAST AS BIPOLAR/81

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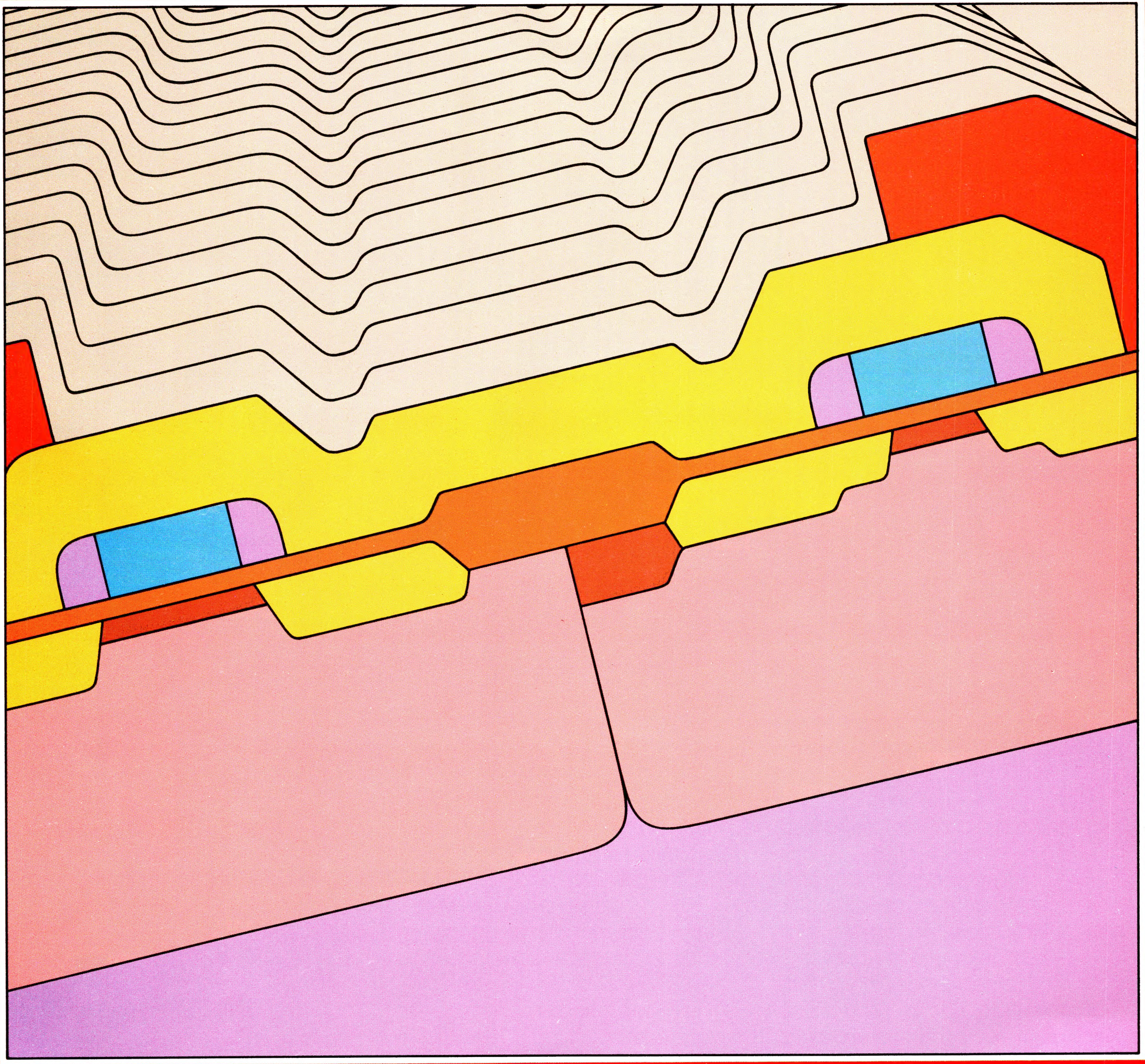

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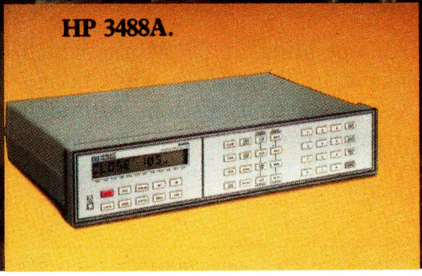
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Next ElectronicsWeek

Consumer products are coming together

The final installment in the Technology Update series will cover the wide spectrum of consumer electronics. Integration is the watchword, and the distinctions between categories—audio and video, for example—are beginning to erode. The frenzy over integrated circuits that overtook the consumer world in the early 1980s died down in 1984. In its place came a wait-and-see attitude as manufacturers shifted from a strategy of packing as much new technology as possible into products to a realization that most consumers are not buying for technology alone. David M. Weber and Wesley R. Iversen collaborated on this report, coming in next week's *ElectronicsWeek*.

The personal computer as a spectral analyzer

Real-time spectral analysis is migrating to the personal computer realm. The necessary hardware is already available, together with some of the software. Additional software is under development, and is contributing to the growth of this engineering application for personal computers. A prospective user of such a system needs to be apprised of the capabilities and limitations of personal computers for spectral analysis. Read next week's detailed look at this newest twist for personal computers.

Looking ahead in ElectronicsWeek

A surprisingly simple local network

A novel local network has been developed, operating at 50 Mb/s, which satisfies the demand for faster and more efficient local networks while taking advantage of the well-known benefits of fiber-optic transmission. Although contention-based, it operates in a collision-free environment, is configured in a rooted-tree topology, and uses point-to-point fiber-optic links. It will be detailed soon in an upcoming *ElectronicsWeek.*

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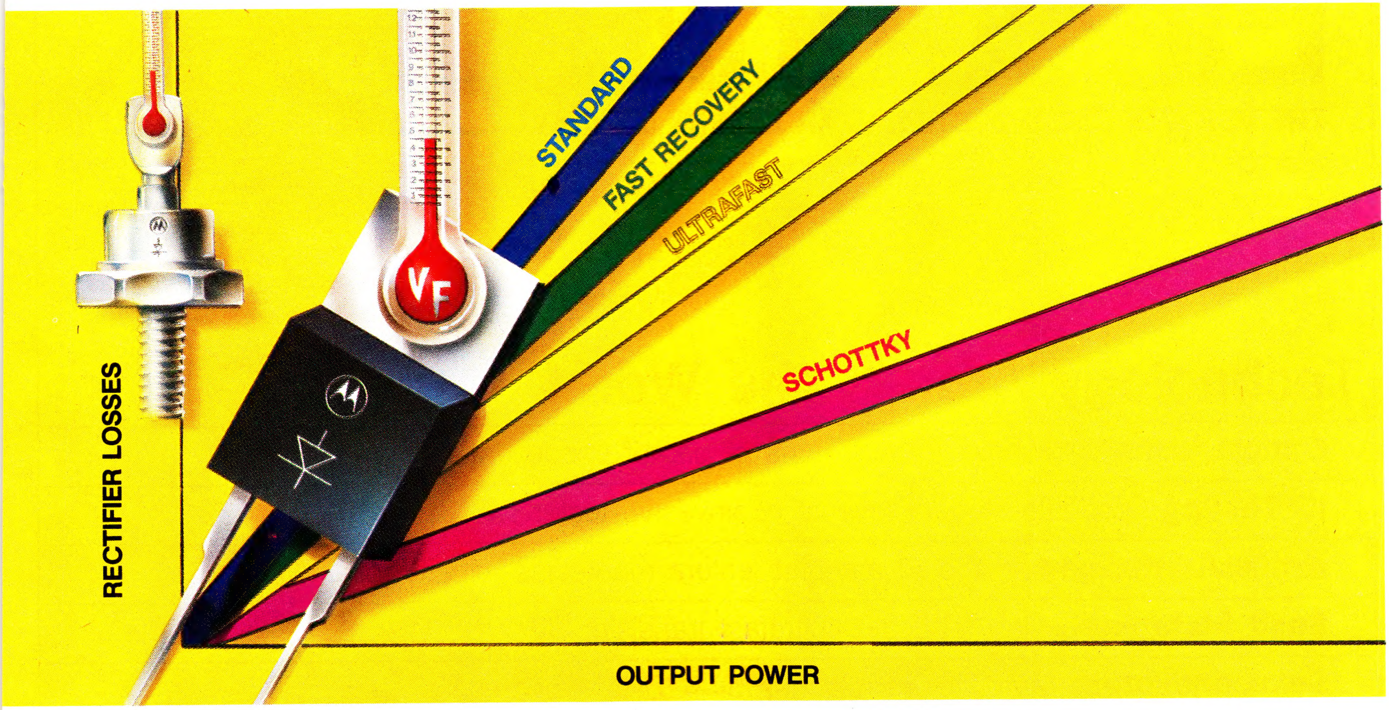

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Packaged in TO-220, the 10 Amp MBR1060 Schottky offers 0.7 V_F and less than 6% power loss, or 94% efficiency, at 120 W P_O. Ordinarily, you'd lose twice that with a slower rectifier, up to now your only choice for higher output power applications. With the MBR1060, you gain the same advantages for 12 V supplies as you've enjoyed with Schottkys in 5 V supplies.

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Axial Lead Glass	0.5	30, 40 V
Axial Lead Plastic	1.0, 3.0 A	20, 30, 40, 50, 60 V
Axial Lead Metal	5 A	20*30, 40 V
TO-220	7.5, 10, 15^+, 16, 20^+, 30^+ A	35, 45, 60 V
DO-4	15, 25*35 A	20, 30, 35, 40*45 V
TO-3	30 A	35, 45 V
DO-5	40, 50, 60, 65, 75, 80 A	20, 30, 35, 40 45 V
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ATE COSTS CLIMBING

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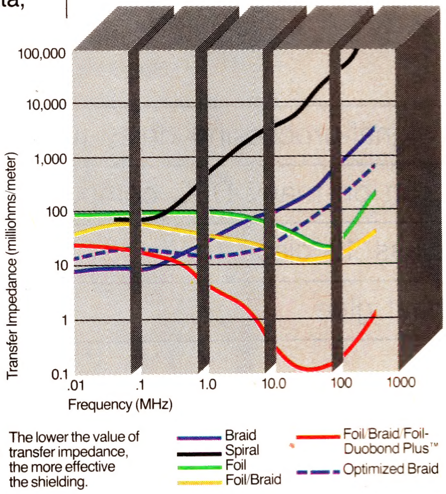

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ElectronicsWeek

Special Technology Reports

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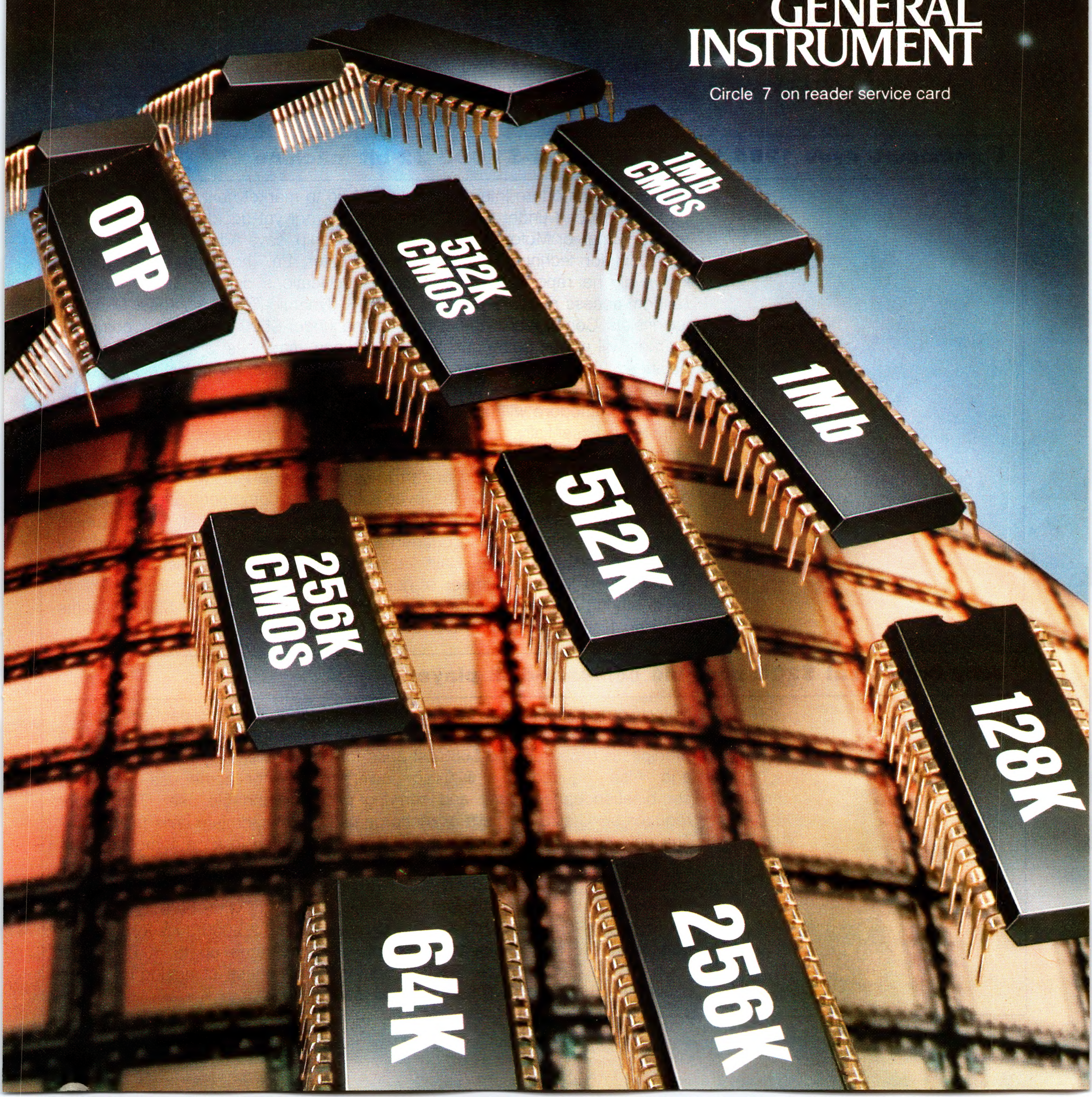

UP FRONT

Honeywell to enter merchant market with CMOS gate array

Honeywell Inc., Minneapolis, already an emerging player in the merchant market for bipolar gate arrays and other devices, is also pushing to enter the market for CMOS gate arrays. Under an agreement with ETA Systems Inc., St. Paul, Minn., Honeywell's Semiconductor Group will produce prototypes before year-end of a 20,000-gate CMOS array built using 1.25-µm technology. (The maximum densities currently available on open-market CMOS arrays are about 10,000 to 12,000 gates, based on 2-µm minimum geometries.) First production of the Honeywell HGC20000 will go to ETA for use in its GF-10 supercomputer, a 10-gigaflop, 8-processor machine planned for initial deliveries in 1986. Honeywell also plans to make the new ETA-designed array available to the open market, though the firm will not set a timetable.

Commodore eyes 1985 launch for under-$1,000 32-bit machine

Look for Commodore International Ltd. to go to market next year with a 32-bit computer priced under $1,000. The firm has not yet decided whether to turn to Zilog, Intel, or Motorola for the processor chip, says Adam Chowaniec, vice president for technology at the West Chester, Pa., home computer maker. However, he reports the preliminary specifications call for 512-K bytes of random-access memory built out of 256-K dynamic-RAM packages. Chowaniec insists Commodore, the leader in the under-$500 8-bit home computer market, will not be going upscale with the new machines to a different kind of business. The company has no 16-bit entry in mind, he points out, adding, "We are moving 32-bit machines down to domestic applications." In so doing, Commodore will face a different lineup of competitors from what it vies with now. Essentially, four computer makers—Commodore, Atari, Texas Instruments, and Timex Sinclair—had the under-$500 market to themselves during the six-month period ended May 1984. (The last two no longer produce home computers.) In the over-$500 home computer category, Apple, Radio Shack, and IBM have some three quarters of the market, with 25 others competing for the remaining quarter, according to a just-published survey by Dataquest Inc., San Jose, Calif., a subsidiary of the A.C. Nielsen Co. The survey found that the number of homes with computers grew from 6.2% to 9.4% during the six months ended in May 1984, with over-$500 systems clocking faster growth than the lower-priced machines.

Sony brings out $200 portable compact-disk player

Sony Corp. has brought out the world's first portable compact-disk stereo system. In Japan, the new unit is priced at a new low of only about $200, a precipitous drop from the $680 list price for Sony's first product just two years ago. Also required is a $20 ac power adapter for home use or a $40 combination battery pack and carrying case for portable use. (The player requires six C-size dry cells or rechargeable nickel-cadmium cells for power.) The new player, which incorporates technology used in an automobile compact-disk player introduced this summer, can operate at any angle and operates despite moderate motion (but it is not recommended for jogging). The unit weighs just over 1.3 lb and measures about 5 in. wide by 5 in. deep by 1½ in. high. Sony claims to be starting production at 20,000 units a month for both domestic and overseas shipments and will ramp up to 50,000 units soon. To spur compact-disk sales, Sony has cut prices of analog-mastered disks by 8.5% and by 16% for digital-mastered disks.

You Owe It To Yourself To Choose From The Best.

Choosing the right logic analyzer can be tough. But one thing is clear—you want all the advantages you know you can count on from the performance leaders.

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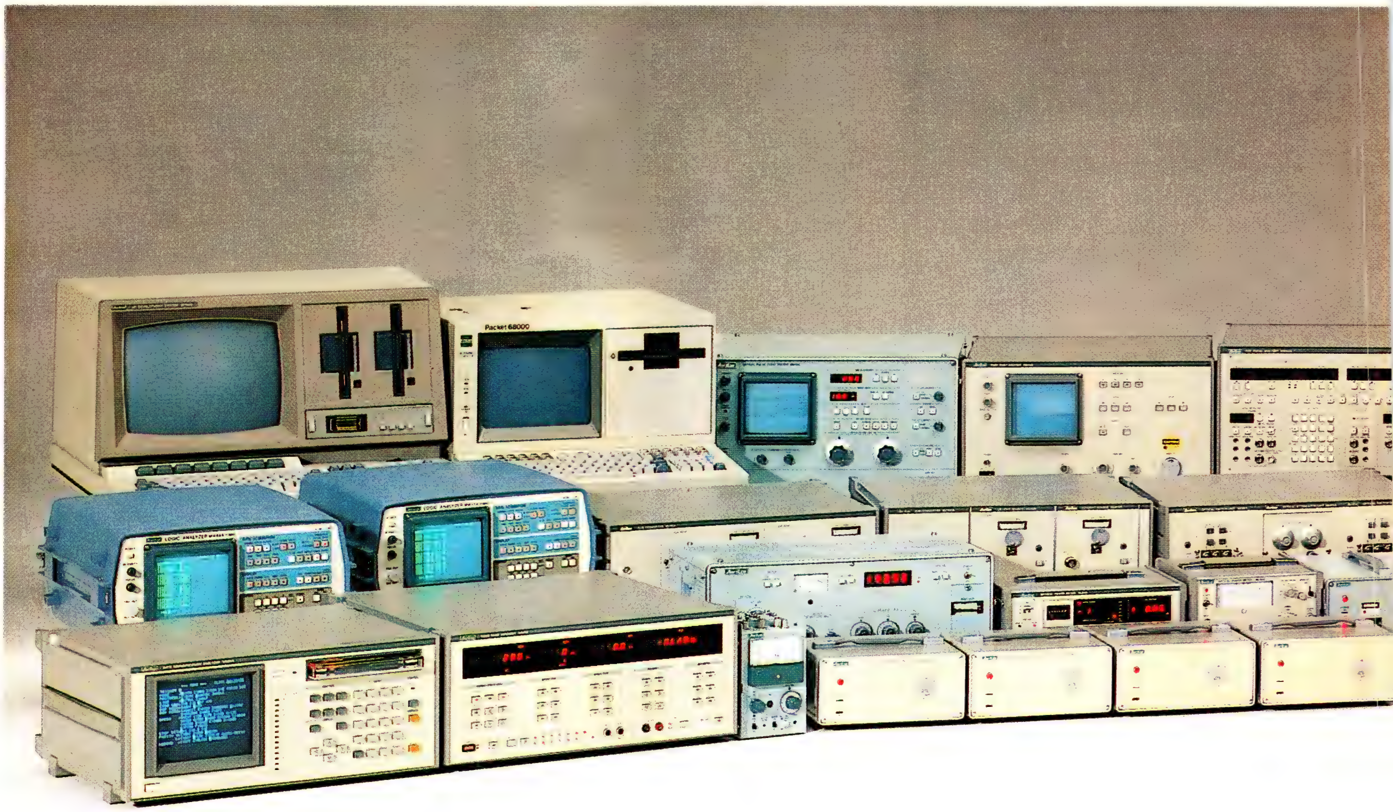
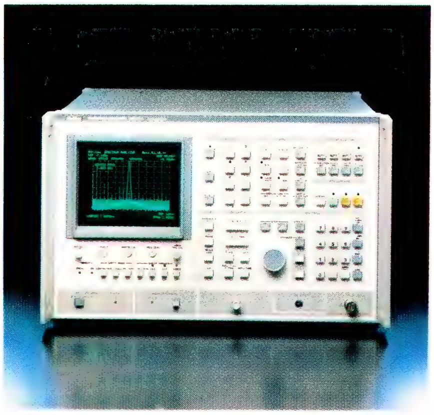


MS611A Spectrum Analyzer
This analyzer covers the range from 50Hz to 2GHz in a single band, and features auto ranging. Resolution bandwidth is 10Hz to 3MHz too. Another better instrument from Anritsu.



Anritsu means communications.

We began building telephone and radio equipment more than 50 years ago. And although we've expanded into other fields since then, we've remained true to those first electronic roots.

In fact, the Anritsu name is now known around the world as synonymous with communications. From public telephones to sophisticated, state-of-the-art

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optical and digital transmission systems, Anritsu communications products are highly regarded for both unequalled reliability and technical excellence.

With such wide-ranging experience in all phases of communications, it's no surprise that our electronic measuring instruments are superior, too.

Anritsu builds the electronic instruments that keep electronic and fiber optic communications operating at the knife edge of efficiency. From the simple measurement of voltage and current to complete high-level analysis of both analog and digital circuitry, Anritsu instruments are built by experts in communications. And Anritsu instruments are built to be used.

Whether it's an Anritsu electronic voltmeter, a network analyzer or a complete GPIB-based automatic test system, you'll find a basic field-proven ruggedness built in. And you'll find controls that actually make sophisticated measurements simpler to perform.

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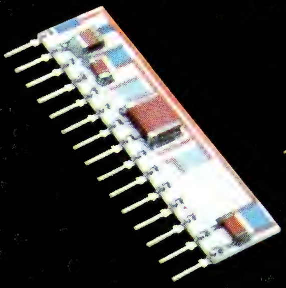
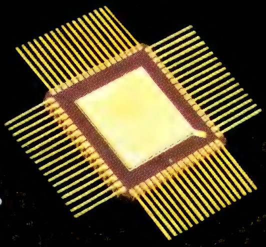
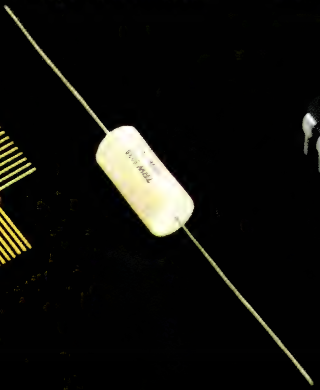
This telephone set filter network is an example of the Resistive Products Division's custom circuits that can include semiconductors, custom linear ICs or any other surface mountable active or passive component.



The TDC1043 multiplier-accumulator from the LSI Products Division operates at a 100ns cycle rate with individually clocked input and output registers and is used in array, video, radio signal, FFT and other digital signal processors.

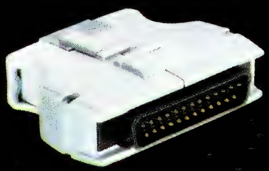


Small precision-wound capacitors that meet the most stringent environmental requirements of the communications market, in film/foil or metallized construction are produced by TRW's Capacitor Division.



Optocouplers from the Optoelectronics Division combine the speed of photodiodes with the reliability of integrated circuits, yet have current requirements so low that they will not load down telephone lines.

This RS232 connector to 8-pin modular jack adapter is an example of the almost unlimited range of telephone adapters and specialized connectors manufactured by the Connector Division for communication applications.



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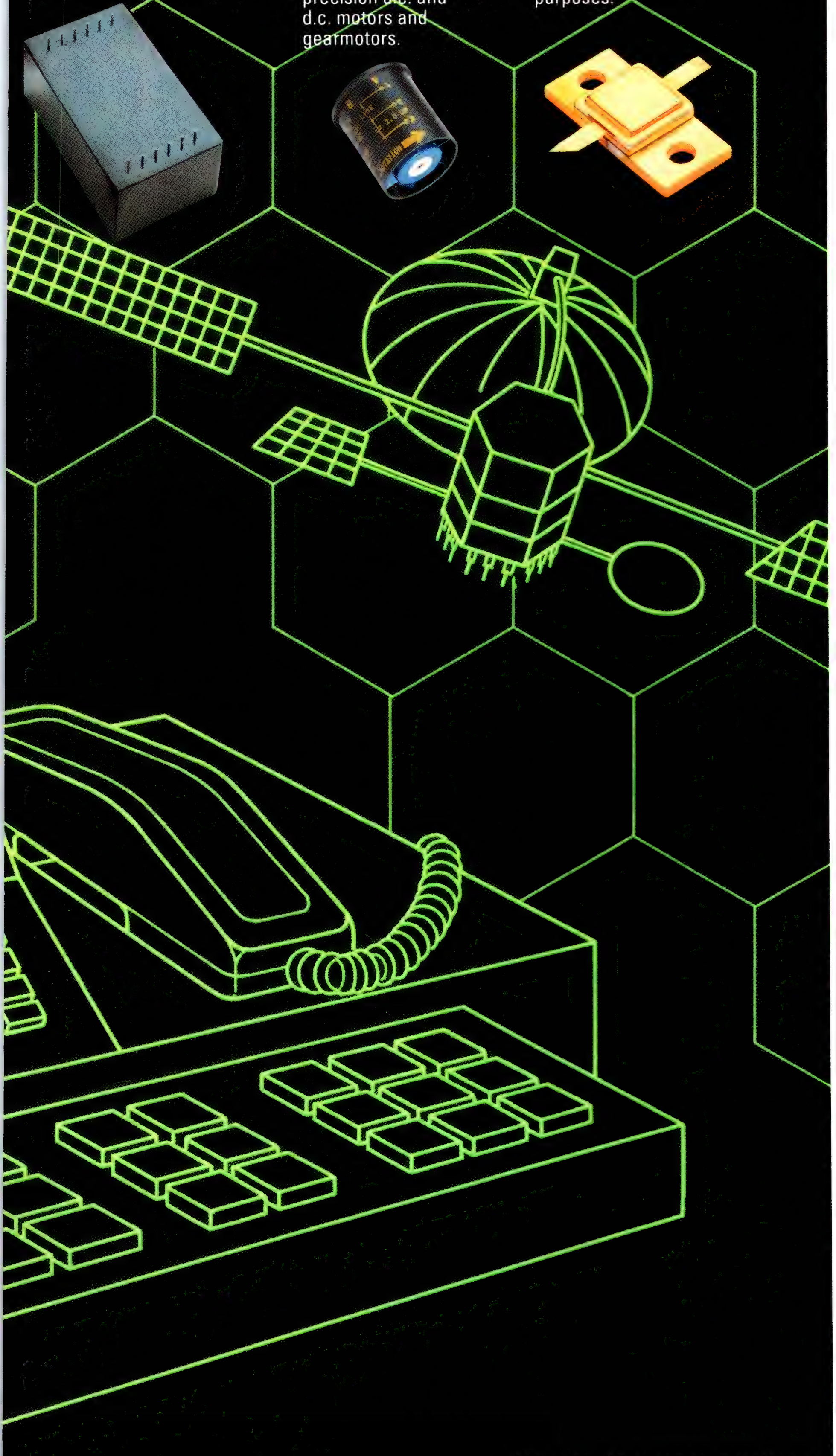
Type MTC telephone interconnect transformers handle up to 120mA unbalanced DC current... representative of the broad range of high reliability products available from the Inductive Products Division.

This fan motor assembly is typical of the high reliability a.c. and d.c. fans and blowers that the Motor Division produces for communications equipment, along with a complete selection of miniature precision a.c. and d.c. motors and gearmotors.

The MRA1214-55H microwave power transistor shown here is rated at 50W CW, 100W pulse, 6.5 dB gain and 1200-1400 MHz. It is representative of the RF Devices Division's products for communications purposes.



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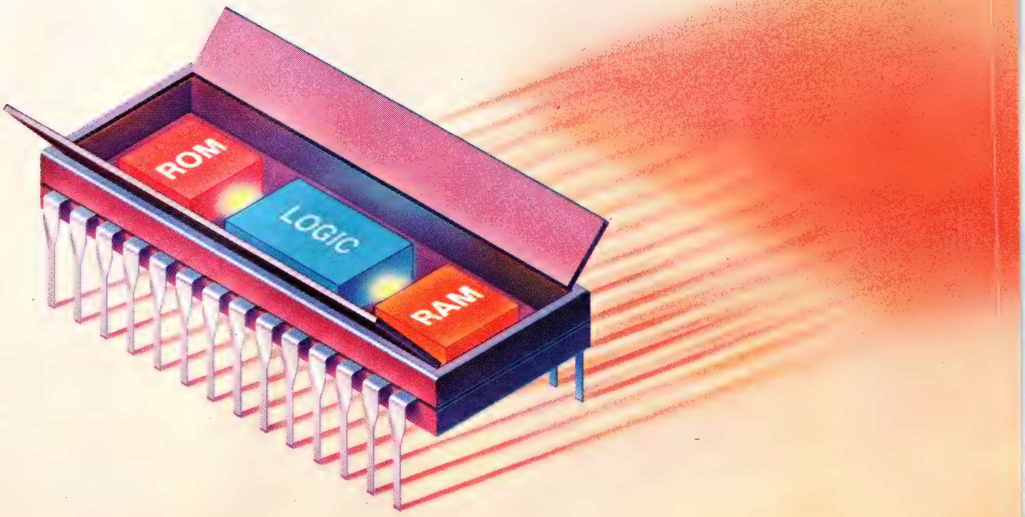

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JUKE BOX STORES TRILLIONS OF BITS OF SPACE DATA

Cornerstone of NASA's archival network stores data on 125 optical disks, ties into fiber-optics bus that runs at 100 megabits/s in bursts

☐ *by Robert Rosenberg*

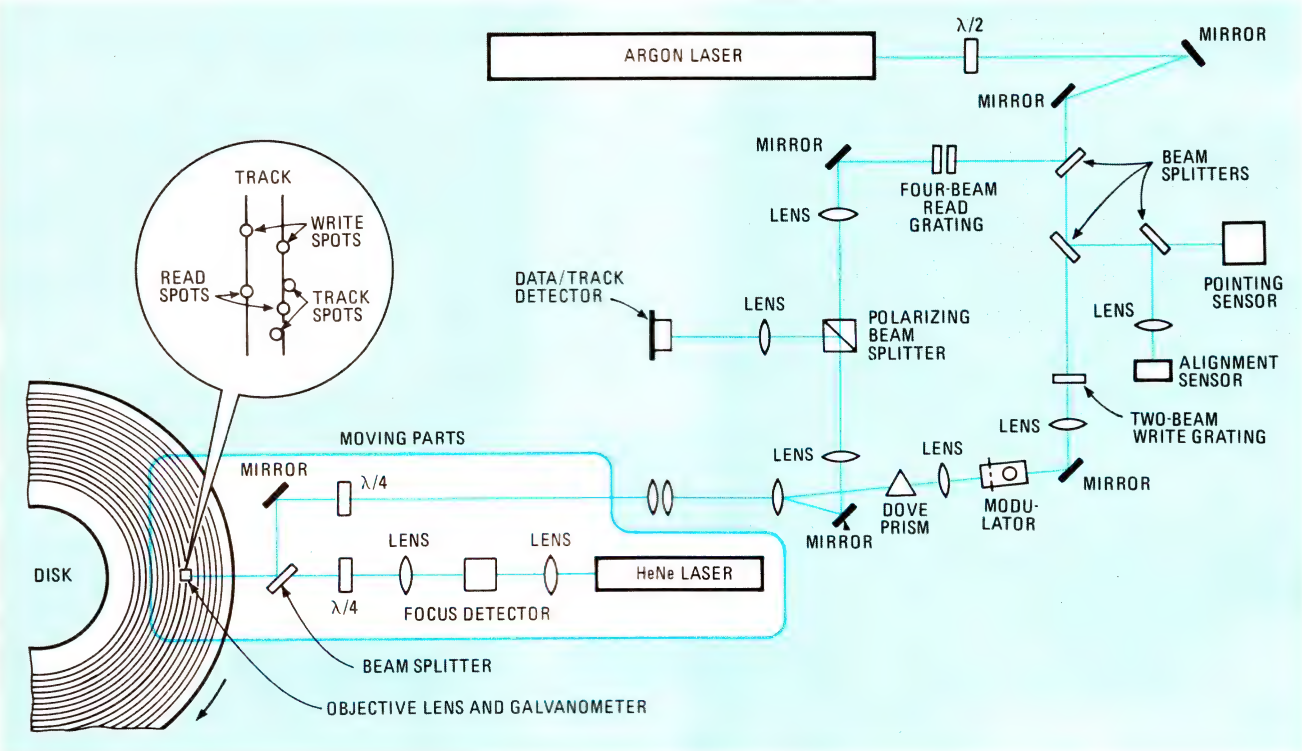
Huntsville, Ala.

A gigantic optical-storage subsystem capable of storing 10 trillion bits is the final building block in a fiber-optic network currently being put together at the Marshall Space Flight Center here by the RCA Corp. Government Systems Division, Camden, N.J. It will link universities and federal laboratories engaged in land-resource, atmospheric, and space-science studies.

The network began to take shape five years ago, after officials at the National Aeronautics and Space Administration realized they were being inundated with data from deep-space probes. As data generated by the probes was amassed, the distribution of computer tapes became enormously time-consuming, says Douglas Thomas, a computer engineer at Marshall working on the installation of the juke box. The Space Telescope, not yet completed, is also expected to add substantially to the volume of data NASA will handle.

To cope with the heavy data flow, NASA planners designed a fiber-optic bus with seven active ports configured in a star that runs at 100 Mb/s in bursts and 50 Mb/s continuously. It links three Digital Equipment Corp. VAX-11/780 superminicomputers that have been fitted with triple-ported memory.

The system was designed with dual paths so that file transfers could take place directly between the juke box and a data source or sink, while



Pair of lasers. RCA's optical-disk juke box has a pair of lasers. The output of the argon laser is split to obtain read and write beams for the twin-track arrangement. The helium-neon laser is the light source for a precison head-positioning system.

control of the transfer remains with the host processor. This architecture frees the control processor from the role of a mere file-switching node and allows it to perform intelligent data-management functions.

Eye-opening capacity. The juke box is the archival system's cornerstone. Each of its 125 fourteen-inch disks can hold up to 10 gigabytes, about 10 times the amount of data stored in most commercially available drives and 2½ times that predicted for the forthcoming high-end drive from Storage Technology Corp., Louisville, Colo., which is still in beta test. In NASA's system, the worst-case access time to any of the 125 disks will be 6 seconds.

Two separate gas lasers are used in the unit. An argon laser is used for read-write operations and a helium-neon unit for the control system that positions the read-write head over the disk.

For data recording, the beam produced by the argon laser, which works at 488 nm, is split to write data into two parallel tracks on the disk at a rate of 67 Mb/s per track (see figure). The beam is passed through a half-wave plate, reflected off two mirrors to adjust positioning, and then split so that a portion of the light is sent to read gratings while the remaining light is split further for writing, pointing, and alignment functions.

The write-phase grating optics split the light further, so that two divergent beams pass to the following lens, which images the spots under the modulator transducer. The diffracted light from the modulator is collimated and sent to a Dove prism, which rotates the image of the two spots and thereby sets the spacing of the tracks formed on the disk. The collimator performs a double function: it enlarges the beams from the modulator enough to fill the objective lens, and it passes an image of the grating—the source of the two spots—to the disk.

Keeping in focus. High-performance servomechanisms are needed to meet the read-error-rate requirements for the minimum recorded feature size of 0.42 μm and the track-to-track separation of 1.0 μm. These servomechanisms control tracking and translation-stage position and keep the objective lens, which is on the translation stage directly above the tracks being written or read, in focus.

The second laser in the system, a HeNe unit, also helps keep the objective lens in focus, providing feedback to the positioning mechanism. To do this, the light from the HeNe laser is first focused, expanded by two lenses, and passed through a two-color beam splitter to the galvanometer and objective lens. Light reflected from the disk returns down the optics chain, and, by action of the quarter-wave plate and beam splitter, is coupled to the focus detector.

Four working beams. For readout, the read beam that is split out of the main argon laser beam is further split into six beams, of which four are used. Light reflected off the disk passes back through the optics and is reflected onto the data/track detector, an array made up of nine avalanche diodes and and four p-i-n diodes. The high-gain avalanche detectors take care of the read signals; the p-i-n detector outputs are fed to the tracking-head control loop.

Using twin tracks for optical storage is still rather exotic. But systems that can write nine tracks in parallel have been demonstrated in the laboratory, points out Jay Hoover, manager of optical recording engineering at the RCA division.

Gigabit bus. While technicians at Marshall work to get the storage system in place, NASA has initiated a series of informal meetings with designers of optical subsytems and manufacturers of supercomputers to begin defining a new standard for a very high-speed data interface. "A new bus interface in the gigabit region is needed, but we don't know how the heck you operate at those speeds," said Ken Wallgren, a NASA data systems manager.

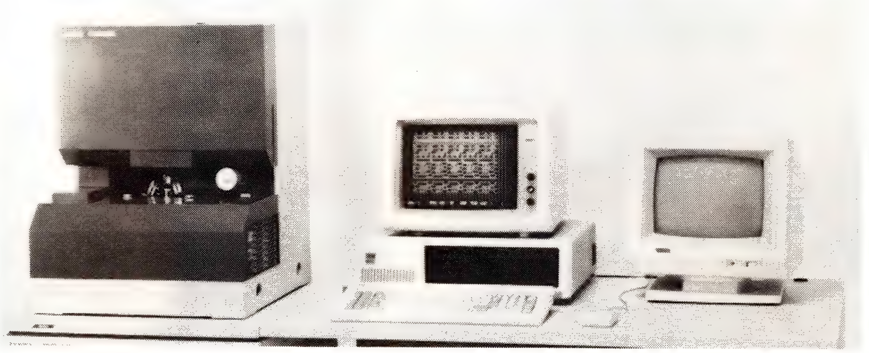
One of the supercomputer manufacturers, Denelcor Inc., Aurora, Colo., says it is willing to work with the agency. "NASA is proposing developing a standard probably so they can mix and match vendors," says Ron Ames, a Denelcor spokesman.

IC TESTING

Graduate student designs noninvasive tester for ICs

Palo Alto, Calif.—A tester that uses a novel laser detection scheme to determine noninvasively the logic state of any node in a complex integrated circuit will be displayed next week at the Institute of Electrical and Electronics Engineers' test conference in Cherry Hill, N.J. Designed by Francois J. Henley, a 24-year-old Canadian graduate student at the University of California at Berkeley, the machine will be built in Japan and marketed by Mitsui & Co., the giant trading firm.

The Data Probe—part IBM Corp. Personal Computer and part optics table containing a laser interferometer controlled by an Intel Corp. 8085



Probing. Designed by a 24-year-old Canadian, the Data Probe uses a novel laser detection scheme to determine noninvasively the logic state of any node in a complex integrated circuit.

microprocessor—operates by using a weak laser probe to induce photocurrents at logic nodes on an IC. Different logic states at the nodes result in different couplings to the power bus.

The system uses a helium-neon laser to induce photocurrents of up to 1 mW, in microwatt increments, in very large-scale ICs. It detects currents on the order of microamperes by means of a process developed for charge-coupled devices. Called correlated doubling sampling, the process measures changes in output values rather than absolute values.

To obtain a precise correlation, the laser is fired in the interval between two time marks. If the window is small enough, noise components in the induced currents are lost in a common-mode signal, Henley says in a paper prepared for the Cherry Hill conference. The laser is clocked at up to 40 MHz in 100-kHz intervals.

Computer processing allows the analysis to be automated. The 1.8-μm laser spot may be positioned by data from a node coordinate file or even from a computer-aided-design data base.

Henley's design grew out of work he had done at Berkeley on the use of a laser in alpha-particle simulation. Donald R. Weeks, president of Spectrum Sciences Inc., a small Santa Clara, Calif., maker of scientific instruments, hired Henley part time to apply the technique to ion implantation. The two abandoned alpha particles for the Data Probe, however, when Henley found that he could devise a method for determining logic states.

Present methods for determining the state of an interior node require clumsy mechanical positioning of a probe, which itself induces capacitative errors in its own measurement. Probing also requires etching away the passivation layer of the chip.

Transparent. The passivation layer is transparent to the laser, and the detection process Henley uses has inherently low noise. The only other noninvasive system (from Integrated Circuit Testing GmbH, Munich, West Germany, a Siemens AG spinoff) uses an ion-beam process [*ElectronicsWeek,* Sept. 10, p. 61].

Last year, Weeks and Henley formed a company called Data Probe Inc. to make the tester, and Weeks, with limited financial resources and manufacturing experience, went looking for a backer. He found that the interested venture capitalists wanted too big a piece of the company for taking a chance with the young firm.

Mitsui, however, had heard about a prototype that Data Probe was showing around Silicon Valley, and sent a VLSI specialist to call on the company. "I thought they could do a better job with the marketing," Weeks says of the Japanese firm, which had 1983 sales of $66 billion.

Mitsui, second only to Mitsubishi in size among Japanese trading firms, accounts for about 10% of all Japan's imports and exports. It has not invested heavily in electronics, but is currently looking at opportunities to do so in semiconductor manufacturing and test equipment.

"Mitsui is putting together U.S. design technology with Japanese manufacturing technology and financial support," says Atsushi Abe, a representative of Mitsui & Co. USA Inc., in New York. "This kind of operation is beneficial to both the U.S. and Japan, and to Mitsui. We are looking for others."

Mitsui provided financing through its U.S. venture fund, and contracted with Anritsu Electric Co., a Japanese instrument maker outside Tokyo, to build the tester, in exchange for a royalty to market it.–**Clifford Barney**

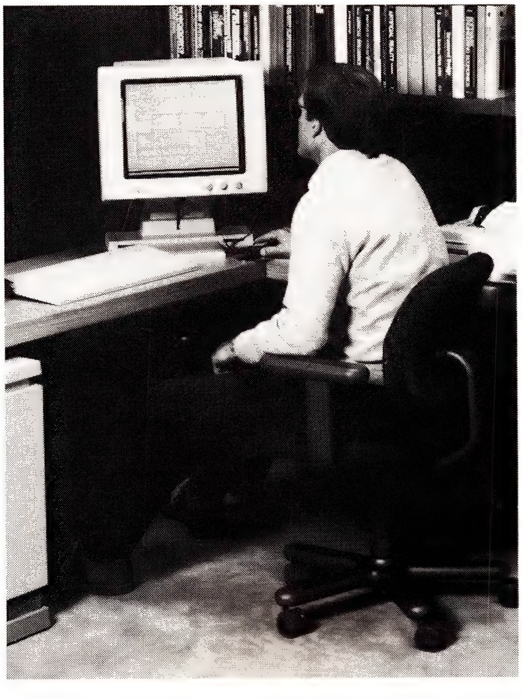
ARTIFICIAL INTELLIGENCE

TI's AI machine enters market already a best seller

Austin, Texas—Texas Instruments Inc. is jumping into the artificial-intelligence hardware business in a big way with a small 32-bit symbolic-processing computer. The Common Lisp-based TI Explorer has been designed to accelerate AI's much-celebrated move out of the laboratory with a cabinet enclosure that is small enough to fit under a desk.

The latest product to emerge from TI's six-year effort in AI research, Explorer is being targeted at a number of research and software-development markets as well as being offered as a low-cost delivery vehicle for powerful AI-based products. Although Explorer is making its public debut this week at the Association for Computing Machinery's Fifth-Generation Challenge meeting in San Francisco, the big splash actually took place over the weekend, when Massachusetts Institute of Technology announced it will buy up to 400 TI systems in the next two years.

Believed to be the largest order ever for AI hardware, the purchase is being made by MIT's Laboratory for Computer Science, in Cambridge, Mass., which plans to fill the center with Explorers and give its researchers a new standard processing envi-



Small wonder. TI's entry into the AI market is the Explorer, a 32-bit symbolic-processing computer with an enclosure that is small enough to fit under a desk.

ronment. "I hope it will revolutionize the way we conduct research and live," states Michael L. Dertouzos, director of the MIT lab.

Explorer will not just process Lisp. In addition, its communciations capabilities will be used to tap many of MIT's research resources, including the new expert-system very large-scale-integration design facility under development at the computer lab, and a multiprocessor emulation facility being built for the Pentagon.

Baby boom. TI's 10-month-old Advanced Systems Division here hopes the MIT purchase—valued at up to $20 million—will send shockwaves throughout the still-infant $100 million AI industry. "We believe the market is now at the point where it will double in size each year for the rest of the decade," says Stephen A. Latter of TI's advanced systems marketing arm.

Touted as a single-user personal Lisp computer, Explorer enjoyed an inside track when competing for sales at MIT. The school's lab pioneered much of the system's technology, including its processor-independent 32-bit synchronous system bus, called NuBus. "All of the concepts we developed—Lisp in 1959, the Nu Machine in the late 1970s, distributed processing, and the Lisp Machine by MIT's Artificial Intelligence Lab—are coming back to us in a well-engineered product from TI," adds Dertouzos.

In addition to the MIT-developed technology, TI has applied its own semiconductor and packaging know-how to reduce the size and cost of symbolic-Lisp processing. Relying on surface-mounting chip technology, the guts of TI's Explorer are packed inside a seven-slot NuBus chassis. Surface-mountable J-leaded chip carriers are used to place 2 megabytes worth of 64-K dynamic random-access memory on a 14½-by-11-in. Eurocard form factor. When 256-K DRAMs are used, TI will offer 8 megabytes of solid-state storage on each board. The Explorer can house two main memory cards.

Based on surface-mountable advanced Schottky bit-slice circuits, Explorer's Lisp processor resides on two piggybacked boards that slip into one NuBus slot. The 32-bit engine contains 16,000 52-bit words of writable-control microprogrammed storage, which is used to speed up Lisp processing. Operating with a 7-MHz clock, the processor runs with a 142-ns microinstruction cycle and can address 128 megabytes of virtual memory with demand paging.

Local bus. In addition to the NuBus, TI has also added a second 32-bit local bus to directly handle high-bandwidth accesses between the Lisp processor module, main memory boards, and graphics bit-map hardware. This helps free the NuBus for system-wide data transfers. The system is also loaded with software enhancements—high-resolution graphics, windows, on-line help, and an optical mouse—intended to smooth things over for the first-time user.

The chassis—about the size of a two-drawer file cabinet—attaches by way of a fiber-optic cable to a 17-in., 1,024-by-808-pixel monochrome display. As does Common Lisp, Explorer contains high-level extensions to the language, such as an object-oriented programming facility, an extensive library of MIT Lisp Machine functions, and loop-macro for simplifying iterative programming steps.

For AI-delivery applications, TI is marketing a low-end configuration at a price of $52,500 with 2 megabytes of memory, 112 megabytes of formatted hard-disk storage, and 60 megabytes of tape-cartridge backup. A stand-alone development system will sell for $61,000 for 2 megabytes of memory, and two 112-megabyte hard disks. In all, the Data Systems Group, in Austin, intends to sell six standard configurations. In 1985, TI expects to expand the list by also offering AT&T Bell Laboratories Unix operating system on Lisp computers. **–J. Robert Lineback**

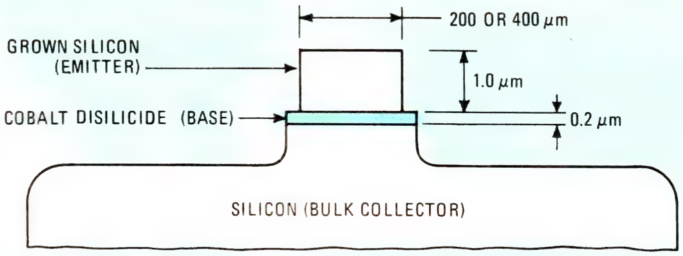
SOLID STATE

French engineers fabricate an ultrafast transistor

Grenoble, France—A team of French engineers at the microelectronics research center of the Centre National d'Etudes des Télécommunications has successfully produced a monolithic semiconductor-metal-semiconductor transistor, a feat that has eluded researchers since such a structure was proposed as a faster alternative to the conventiononal all-semiconductor npn transistor more than two decades ago.

Their prize is a device that substitutes a very thin layer of metal for the base of a standard transistor. Thus it all but eliminates performance limits dictated by the resistivity of a standard transistor's base while dramatically reducing the transit time necessary for electrons to travel from collector to emitter. The theoretical cut-off frequency for optimized SMS transistors, researchers at AT&T Bell Laboratories have calculated, should be something like 30 GHz, faster even than gallium arsenide devices.

Structurally, the SMS transistor is deceptively simple: it is formed by a thin layer of cobalt disilicide sandwiched between two thicker layers of silicon. In operation, the silicon lay-



Fast sandwich. A very thin layer of cobalt disilicide sandwiched between layers of undoped transistor gives a transistor that theoretically could operate at 30 GHz.

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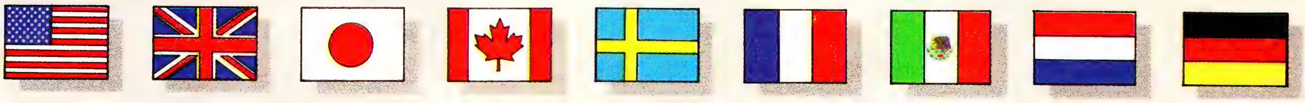

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Circle 22 on reader service card

ers serve respectively as the transistor's emitter and collector, on opposite sides of the $CoSi_2$ base.

Engineers have for years been carrying out experiments on the characteristics of such structures using unstable configurations where, say, semiconductor needles or small specks of semiconductor serve as emitters. But only recently has the fabrication of a monolithic device been considered possible.

Pair of barriers. Holding back such a realization were two stumbling blocks. First was the availability of a vacuum perfect enough to prevent pollution of silicon grown on metal. Trying to grow silicon on metal in a standard 10^{-6} torr vacuum yields a layer of impurities mixed with crystal within one second. That problem can now be resolved by ultravacuums at 10^{-9} torr for molecular beam epitaxy, which provide an almost leisurely hour for the growth of the a 1-μm layer.

The second snag was to find the right metal, a silicon compound with a metallic crystal surface suitable for the epitaxial growth of silicon crystals. The CNET capitalized on work done at Bell Laboratories and Japan's Nippon Telephone and Telegraph Public Corp. and chose $CoSi_2$ because of its lattice mismatch of only 1.4%, compared with single-crystal silicon. Both Bell and NTT have teams working on SMS projects, though neither has realized a working transistor, CNET claims.

Triple layers. Fabrication of the device begins with a standard silicon substrate that goes through a rigorous cleaning process, after which a layer of cobalt 65 Å thick is deposited by evaporation. Annealing this layer at 650°C yields a film of $CoSi_2$ 200-Å thick. A 1-μm layer of undoped silicon is grown atop the $CoSi_2$.

From this structure, square Schottky diodes, either 200 μm or 400 μm on a side, are defined by reactive ion etching of the upper silicon layer down to the level of the $CoSi_2$. CNET says it has mastered this critical step, where the etching must be stopped within the $CoSi_2$ layer's 200-Å thickness. The Schottky diode between the metal and the bulk silicon substrate is then defined using standard photolithographic techniques to get a double-mesa structure (drawing). Contacts are realized with standard wire bonding.

In the euphoria of being first to have realized a monolithic SMS transistor, the CNET researchers haven't lost their sense of perspective. "There's a long, long way to go in making SMS a standard technology. That will take many years," admits Emmanuel Rosencher, one of the CNET engineers working on the project. "We're at the same point now with SMS as we were 20 years ago in the development of the standard transistor."

Still, there are potent reasons for optimism. The device operates at room temperature and gains little in performance from cooling. Besides reducing base resistance and electron transit time, it virtually eliminates minority storage delays. And perhaps most important, the structure is simple, the fabrication techniques standard, and it is entirely compatible with MOS.

Having cleared the first hurdle, CNET researchers will now try to improve the transistor's operation. First steps will be to reduce the thickness of the metal layer and to explore the effects of doping on the silicon layers. **–Robert T. Gallagher**

SEMICONDUCTORS

Firm cuts prices of 64-K DRAMs

Boise, Idaho—The pipeline in personal-computer components may be backing up for at least one supplier, and others are hoping to be spared any repercussions.

Micron Technology Inc., a semiconductor maker here, has cut prices on two of its 64-K dynamic random-access memories to under $2. (The firm won't say what the old prices were, but sources peg them at about $3 per chip.) Micron says the prices were reduced—to $1.95 for a 150-ns 64-K and to $1.85 for a 200-ns chip—because it is trying to boost its U.S. market share and break into the Far Eastern market.

Micron Technology is a leading supplier of 64-K DRAMs for non-IBM Corp. personal computers, a business that has seen better days. The firm also has a new chip-fabrication unit coming on stream and it must find new customers to soak up the excess. However, one vendor suggests Micron is in trouble with its next-generation 256-K design and the price cuts are a ploy to delay implementation by users of 256-K chips.

Price war. The Micron Technology pricing is "the opening salvo of a pricing war. The only difference is a U.S. company fired the first shot this time," maintains market analyst Will Strauss, a vice president at In-Stat Inc., Scottsdale, Ariz. Several months ago, In-Stat president Jack Beedle predicted that 64-K DRAMs will sell for $1.50 before the end of the year.

Still, merchant chip suppliers are downplaying the pricing move by Micron Technology and are vehement in their views that 64-K DRAM prices are firm. The Micron pricing is for slow, low-quality ICs, maintains Steven Lau, a director of Fujitsu Microelectronics Inc., Santa Clara, Calif. "I don't think going below $2 is called for."

Fujitsu is negotiating with customers for next year's 64-K DRAMs, he says, and it expects the price for high-quality high-speed circuits to be close to $3 by the first quarter of 1985, and possibly in the around $2.50 by the fourth quarter. "That is nowhere near where Micron is quoted, and we have no intention of chasing after them," Lau says.

Hitachi Ltd., San Jose, Calif., has been selling its 64-K DRAMs for over $3 and it sees no reason to change that price, a spokesman says. In fact, he adds, the fastest chips are selling at close to $3.50.

"In the industry, we're going to have to wait and see" about price changes, notes a spokesman for National Semiconductor Corp. at its West Jordan, Utah, facility. The firm's production of 64-K DRAMs is booked through May 1985 at close to $3.

Sources at semiconductor firms in Japan doubt seriously that Micron Technology can sell even at its new prices, especially in the Far East. "This strategy is ludicrous," says an electronics component importer who asked not to be identified. "You just don't drop into the Japanese market and start selling at lower prices. Account loyalty is very strong here.

"Changes only develop over time. Some new company coming in with lower prices is not going to have any major effect on the market price here," he adds.

A recent survey by Sumitomo Bank estimates that overall Japanese semiconductor production for the current fiscal year ending next March 31 will be 68% higher than a year ago, with no serious weakening in demand until the last two quarters of 1985. **–Robert J. Kozma**

CAREERS

NSF sees scant shortage of EEs

Washington, D.C.—The National Science Foundation has come up with ammunition for both sides in the long-standing debate over employment prospects for electrical and electronics engineers and computer scientists. In a just-out report, the first authoritative government study on the issue, the NSF projects a shortfall by 1987 of from 115,000 to 140,000 computer specialists and an unmet demand for EEs that will reach 10% of the supply—about 30,000 people.

But the report also concludes that occupational mobility—shifts of engineers from other specialties into electrical and electronics occupations—plus incoming university graduates and immigrants, will just about wipe out the natural shortfall. These conditions will combine to slash the potential shortfall for computer scientists to between 9,000 and 11,000 and send the shortage of EEs tumbling to only about 1,000, the NSF figures.

Same ballpark. The raw numbers fall in the same ballpark as projections made by the American Electronics Association, which has been warning about a shortage of engineers in recent years. "In the NSF report, we see a realistic coming together of all the different demand scenarios," notes Pat Hubbard, AEA's vice president of engineering education.

But NSF's and AEA's positions on the supply side are a different story, she quickly adds. "AEA believes that occupational mobility is healthy and will occur but it will not solve the shortage as NSF so encouragingly suggests."

First, in an economy marked by rapid growth, including defense, AEA questions how many non-EEs will truly be available for occupational crossover. Moreover, high defense spending will make for a very tight labor market. Under such conditions, defense employment of new EEs will increase twice as fast, to 9% between 1982 and 1987, as civilian employment, reports NSF. Aggravating the situation is the fact that military requirements tend to be ones "that either demand highly specialized skills or are fields that currently have undergone shortfall in supply," concedes the study.

Second, even if occupational mobility does ease shortages, it will be at a cost that offsets the gains, posits Hubbard. Turning a hard-core physicist into a computer programmer takes time and money. The enormous retraining effort required to bring supply and demand into balance "will sap the productivity of American electronic companies and hurt their ability to remain internationally competitive," she argues.

More significantly, the issue is not just numbers, claims Hubbard. Disturbingly, the trend appears to be toward improving quantity at the cost of worsening quality, claims Hubbard. Last year, EE departments produced 18,590 BSEEs, about 2,000 more than AEA had anticipated. At the same time, the Accreditation Board for Engineering and Technology gave accreditation to only 35% of the 353 departments it examined. From 1978 to 1983, the number of departments that received the board's stamp of approval declined by 50%, she says.

Fellowships. The quality problem stems from student-to-faculty ratios and is further exacerbated by a shortage of current teaching equipment. While firms are calling for boosting production of engineering students, they are now saying that efforts to upgrade the quality of their training must be given equal priority. This year, AEA members will donate over $7 million to support fellowships aimed at building up faculty on college campuses, reports Hubbard.

Heightening its concern over quality and a matching level of commitment to do something about it is a good measure of how much faith the electronics industry has in the NSF's treatment of the supply side of the problem, she suggests.**–Karen Berney**

LEDs

Silicon carbide ends long quest for blue light-emitting diode

Munich, West Germany—Despite years of research and development in Europe and Japan, the blue light-emitting diode has remained an elusive component, barely getting beyond the sampling stage. Besides some inherent physical problems, what has kept blue LEDs from going into volume production has been the difficulty of processing, at reasonable cost and yield, the semiconductor materials that exhibit the large band gaps needed for blue light radiation.

But now, after a decade of trials and discarded approaches (see "Long search for elusive blue," p. 29), Siemens AG of West Germany thinks it has the fabrication process well in hand. The firm has announced that it will start volume production of blue LEDs by early next year, adding them to its line-up of red, orange, yellow, and green LEDs.

Marketing people at the Munich company see enough applications ahead to justify that move despite the LEDs' high cost: blue LEDs are over 100 times more expensive than diodes emitting other colors. The company expects to sell them for be-

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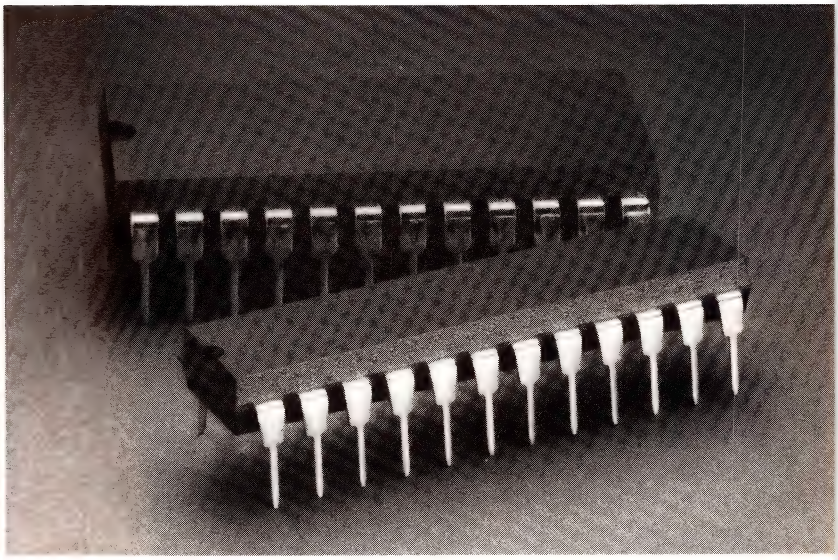

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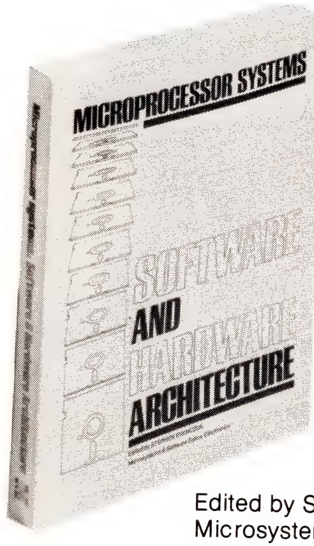

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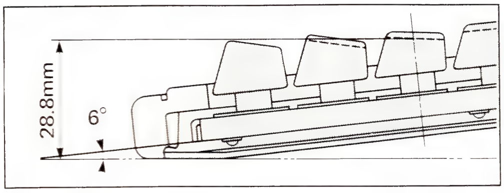

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Long search for elusive blue

In their research efforts on blue light-emitting diodes, the experts at Siemens AG started 10 years ago with gallium nitride as the base material. But with this material it proved impossible to produce the p-n junctions that are necessary for the low forward voltages that allow pulsed operation. Investigations then focused on zinc sulfide and zinc selenide. But with these materials, p-n junctions are difficult to produce. According to Siemens, at least one Japanese producer—Matsushita Electrical Industrial Co.—tried to get around this drawback by using gallium nitride and a metal-insulator-semiconductor construction for their blue LEDs.

"We then turned to silicon carbide and have become convinced that this is the best material for a blue LED," says Claus Weyrich, head of applied materials research at Siemens's Central Research Laboratories, in Munich. With this large-bandgap material, p-n junctions can easily be made. Although their light-generation efficiency is lower, silicon carbide diodes have a better injection efficiency, due to the p-n junction, than the other materials. Sanyo of Japan has also reported using silicon carbide with p-n junctions, Weyrich says.

In addition to its blue radiation capability, silicon carbide has a number of other advantages. Among them are its extreme chemical inertness and stability against radiation, its high dielectric strength—it is 10 times higher than that of silicon—and its high thermal conductivity. Further, the material has been successfully tested for operation at temperatures that have exceeded 500°C. It is for these reasons that the Siemens researchers are also looking at silicon carbide as a possible base material for high-temperature devices such as sensors. "So we are using the blue LED as a vehicle for further silicon carbide device development," Weyrich notes. **–J.G.**

tween \$16 and \$30 apiece, depending on quantity.

There are, however, "professional uses where price is often not a deciding factor," according to Helmut Kindl, marketing manager for optoelectronic components. He offers such applications as light sources in medical equipment (to test the human eye), spectroscopy, calibration light sources in photography and TV cameras, and smoke detectors.

The base material for the Siemens product is silicon carbide, "a material that we . . . found to be the best for blue LEDs," says Claus Weyrich, head of applied materials research at the firm's Central Research Laboratories here. With it, p-n junctions are easy to make. Further, silicon carbide is chemically inert and stable, has a high dielectric strength, and can be used in high-temperature environments.

Drawbacks. For all its advantages, however, silicon carbide has some drawbacks. Because of its high chemical stability, fabrication processes at much higher temperatures than those required for silicon must be employed. Also, because silicon carbide cannot be melted at easily manageable pressures, it is difficult to get the large-area substrates needed for economical device fabrication.

But by using an optimized sublimation growth process with controlled condensation of silicon carbide on a seed substrate, Siemens researcher Günther Ziegler managed to grow silicon carbide ingots large enough to be useful as substrates. Wafers are cut from ingots about 15 mm in diameter and 20 mm long.

The preproduction blue LEDs Siemens has made have a typical luminous efficiency of 10^{-2} lumens/W. Efficiencies four times better were obtained with lab-produced diodes, which, Weyrich maintains, is the highest efficiency value reported so far for a blue LED.

The peak wavelength is 475 nm; the dominant wavelength is 480 nm, which gives a pure blue color impression. A narrow spectral bandwidth, from 50 to 100 nm depending on the diode current, ensures high color purity. The forward voltage at 20 mA is 4 V. At 20 mA, the brightness is around 4 millicandles at a half-intensity angle of 16°.

The p-n junction, together with a low series resistance, makes the LED suitable for pulsed operation. As for degradation, "we are confident that it will be almost negligible," Weyrich says.

Researcher Ziegler performed the ingot growth in a reaction chamber consisting of an outer cylinder of electrographite and an inner cylinder of porous graphite. The lower part of the space between the cylinders is also filled with porous graphite. The upper part contains undoped as well as aluminum-doped silicon carbide powder.

A seed substrate about 10 mm in diameter from a silicon carbide crystallite is placed at the bottom of the chamber. Under high temperatures, the silicon carbide powder sublimates and condensates on the seed, leading to the growth of a single-crystal aluminum-doped silicon carbide ingot. The growth temperature, obtained by radio-frequency heating, is around 2,200°C and the temperature gradient 10°/cm to 25°/cm towards the seed.

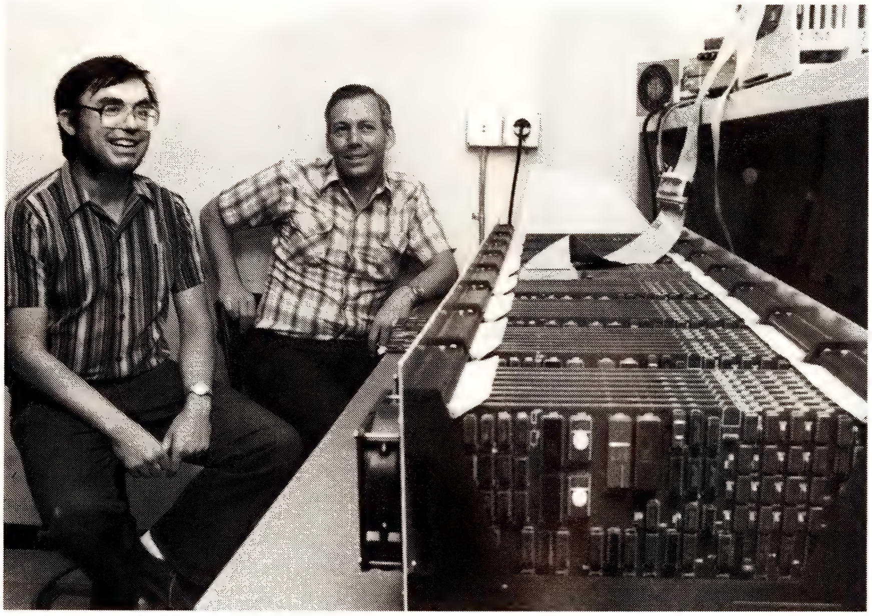
"Growing silicon carbide ingots of the dimension we have obtained—15 mm in diameter and 20 mm long—may not sound exciting to those specializing in pure silicon, but to those familiar with the difficulties silicon carbide presents, growing ingots of that size is a big achievement," Weyrich notes. "It is a prerequisite for mass production of blue LEDs."

The trick in material processing, he points out, is to get the right hexagonal crystal structure. Essentially, this is obtained by careful selection and control of the growth temperature. **–John Gosch**

COMPUTERS

Caltech project scores points

Pasadena, Calif.—Although it is taken for granted that concurrent processing is a cinch to make a big splash as a practical computing technique for small computers, that moment has so far largely eluded a worldwide army of researchers. Stumbling blocks start with melding standard components into a workable architecture. Further, little work



Ruminating. Geoffrey C. Fox, professor of theoretical physics (left), and Charles L. Seitz, associate professor of computer science, watch the Cosmic Cube, an experimental concurrent processor that has been running for the past year at Caltech.

other than simulation has been done toward writing the software that can exploit the advantages of concurrency, which attacks a problem by breaking it into segments that can be solved simultaneously. Today's computers must run programs in sequence, thus more slowly.

An experimental program up and running at California Institute of Technology is therefore gaining widening attention in computing circles. It consists of an array of 64 microcomputers, termed nodes, organized so their separate computations can be coordinated by messages passing through a network of communication channels.

Called the Cosmic Cube by developer Charles L. Seitz, associate professor of computer science, and his students, the machine in its present form is packaged with one node per circuit board, taking up about five feet of a laboratory desk top. The Caltech computer consumes 700 W and costs about $80,000.

Out in front. Though there are now about 150 research programs underway worldwide in the race to build a working concurrent computer, the Caltech program seems to have opened up daylight over its rivals. The noteworthy achievement: "We have been operating the Cosmic Cube since October 1983, so Caltech scientists can develop application programs for it," explains Seitz.

The experience of running practical computing programs for a year has pointed up the advantages of the concurrent machine, which "clearly demonstrates its cost-effective technology," according to Seitz. In speed, application programs are executed at up to 3 million 32-bit operations/s, which makes it about one tenth as fast as a Cray-1 supercomputer for the same problems. Compared with a Digital Equipment Corp. VAX 11/780, the Caltech computer with its 64 nodes can run at best about 10 times faster.

For instruction processing, the Cosmic Cube uses an Intel Corp. 8086, which was the only single chip with a floating-point coprocessor when the processor was developed. (Intel donated the chips for the first machines; the overall research was sponsored by the Defense Advanced Research Projects Agency.)

Each node has 128-K bytes of dynamic random-access memory storage. Seitz notes that in 6,000 hours of operation, the machine had only two hardware failures, both of which were quickly repaired and did not cause any operating problems. Fault-tolerance is inherent in the processor's architecture, he points out.

Probably the most eye-opening part of the Caltech program is how researchers have dealt with the lack of algorithms specifically written for concurrent operations. Seitz, in fact, observes that pulling off this feat is probably too difficult to make the effort worthwhile at present. Instead, the process code necessary for the computer is written in a familiar language—"Take your choice, whatever works," advises Geoffrey C. Fox, professor of theoretical physics—compiled on a conventional computer, simulated, debugged, and loaded into the unit. A kernel operating system installed in each node provides a practical applications environment, based on a message-passing communications scheme.

What has been learned by working with the Caltech processor barely scratches the surface on concurrency, and work on more advanced versions is underway. For his part, Seitz is leaving simple hardware improvements to others and concentrating on a single-chip version of the process node. The design is completed for this Mosaic project and prototype machines should be ready during this school year.

Speeding up. Meanwhile, Fox is working with the Caltech-affiliated Jet Propulsion Laboratories in the construction of a 128-node computer, which is aiming for a threefold improvement in speed over the existing machine. The new computer is about a quarter of the way to completion. Fox also plans to document the program with tutorials and handbooks.

Word of the Caltech project is spreading, for its low-key phase is ending. At Denelcor Inc., Aurora, Colo., its progress is welcomed, says manager of market development R. David Lowry. "There's room for all levels of concurrency and parallel computing. It's easier and easier to prove the advantages." Denelcor's Heterogeneous Element Processor is a leading supercomputer of this type, with its smaller version—a machine processing 10 million instructions per second—going for some $1.3 million.

The commercial potential of the Caltech work has not gone unnoticed, and the school has licensed it to a large computer vendor. Terms of the agreement prohibit Caltech people from discussing plans, because this unnamed firm wants maximum impact from a product announcement coming later this year. Seitz, however, notes that first computers could be available for sale as early as 1985. **–Larry Waller**

Versatile digital adaptive filter uses cascading to attain 960 taps

Martlesham, England—Adapative filters may soon pioneer such electronics applications as listening to a fetal heartbeat with greater clarity, spotting telltale signs of seismic explosions, or canceling unwanted echoes in loudspeaker telephones. The means is a digital-adaptive-filter chip set developed at British Telecom's Martlesham Research Center.

The center's Adaptive Audio Systems Group has designed a four-chip set in a 3-μm, n-MOS large-scale integrated-circuit technology that it says offers a higher performance and a greater flexibility than anything yet developed. The system consists of two 240-tap transversal filters sharing a common input; its architectural flexibility stems from the fact that it can be cascaded in up to four stages to a maximum length of 960 taps, equivalent to a tap-delay of 120 ms—the critical parameter in adaptive filter design.

Though the adaptive-filter theory was worked out by Bernard Widrow (now of Stanford University) more than two decades ago, practical filter circuits have had to await the emergence of LSI technology. The first breakthrough came in 1980, when Bell Laboratories, in a technological tour-de-force, implemented an adaptive digital filter in a massive (1 cm on a side) LSI chip [*Electronics,* Feb. 14, 1980, p. 147]. The circuit was designed to cancel unwanted echoes in satellite links and long landlines.

Many uses. In comparison with Bell's feat, it might seem that British Telecom's four-chip digital adaptive filter scarcely stretches the LSI state of the art. But the Bell chip was basically designed with one purpose in mind, whereas the digital adaptive filter is conceived as a general-purpose chip set, says Alwyn Lewis, who heads the British Telecom team. It can handle a larger number of filter coefficients than the Bell chip and can be cascaded simply by means of serial data links to over 960 tap delays, further enhancing performance. Basically, the longer the filter delay, the greater the number of potential applications.

British Telecom primarily devel-

Matching signals with an adaptive filter

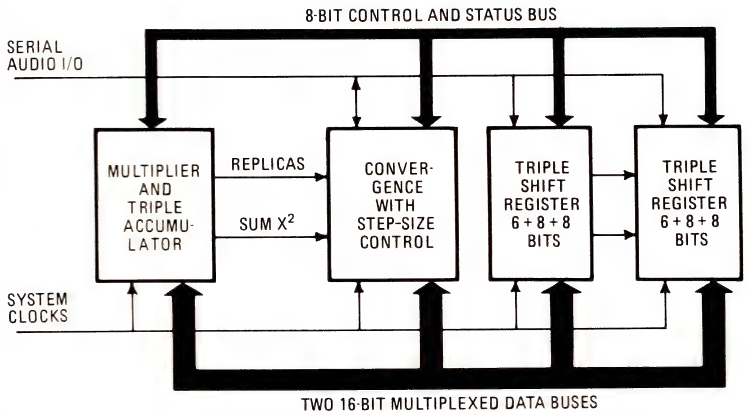
The theory of adaptive digital filtering was first worked out some 24 years ago by Bernard Widrow, now a professor at Stanford University, in Palo Alto, Calif., and M.E. Hoff. They developed the Widrow-Hoff Least-Mean-Squares algorithm, which is now implemented in British Telecom's digital adaptive filter. Adaptive filtering works by reducing the error between a source signal and a corrupted and delayed version of the same signal in a continuous process of statistical convergence.

Its practical implementation on a wide scale, however, has awaited the development of large-scale integrated-circuit technology and suitable digital-filter techniques. Digital filtering essentially adds weighted samples of a delayed signal to the original signal to produce a required output response. In a transverse filter, for example, multiplication takes place after every storage—or tap delay—operation. The tap signals are then summed and added or subtracted from the input signal.

In a conventional or programmable filter, the weighting coefficients are fixed, but in an adaptive filter coefficients automatically adjust to optimize the target signal they are trying to match. Their ability to do so depends on tap length. Generally speaking, the greater the number of taps, the larger the delay a transverse filter can handle.

Any digital-filter function can be built from a multiplier-accumulator and a data store holding data samples and weighting coefficients. In British Telecom's digital adaptive filter, the multiplier chip is a 12-by-16-bit pipelined multiplier-accumulator for convolution and signal-level calculations. It eats through audio-signal data at a rate of 6 million multiplications and additions/s.

The chip set is fed from a 12-bit converter operating at an 8-K sampling rate. Meanwhile, data samples and their respective multiplier coefficients are held in two identical custom-built shift registers, each 5,250-K bytes in size. Two complete transverse filters, sharing a common input, are simulated in this setup by multiplexing between two distinct sets of filter coefficients, interleaved in their common store. The fourth chip in the set dynamically adjusts the coefficients of the filter according to the Widrow-Hoff LMS algorithm. –**K.S.**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oped its digital-adaptive-filter chip set for use in loudspeaker telephones and in audio- and video-conferencing setups where the chip sets could replace conventional voice-activated switches in loudspeaker telephones. The problem with the latter is that they cannot handle simultaneous speech, so conversations are stilted and unnatural. Yet without voice-switching, reverberation would feed back into the phone and cause a nasty howl. A better solution is to use a long-delay adaptive filter to attenuate the direct-coupling between loudspeaker and microphone as well as longer-delay room reverberation that also feeds back into the microphone.

Two filters. In the digital adaptive filter, two filters are driven from a common input signal (see "Matching signals with an adaptive filter," p. 31). One filter is adaptive; the second is programmable, taking its filter coefficients from the first. This ensures that there is always a fall-back set of coefficients. The fast-acting filter can apply 50 dB of echo cancellation at a rate of 165 dB/s. Continuous normalization gives more than 30 dB adaptation over a 30-dB range.

Aside from use in loudspeaker telephones, the chip set can also be used in automatic line equalization (important in data communications applications) as well as in echo cancellation on international calls. Lewis believes that the digital adaptive filter could also find wide application in industrial, biomedical, and scientific signal processing. Such a filter can follow requirements that change or have characteristics of a complexity that defies common filter design.

To obtain this flexibility, Lewis's team has partitioned the design into three functionally distinct chips that can easily be configured, with high yields, to 3-μm n-MOS design rules. The digital-adaptive-filter chip set has been fully custom designed, with part of the layout contracted out to Warmsley Electronics, a custom-design house in Edinburgh, and wafer-processing handled by STC Semiconductors Ltd., in Footscray, Kent. First wafers have now been received. One chip worked the first time; the other two had small layout errors.

So far, British Telecom has not made final marketing arrangements for the chip set, but will likely license manufacturers. –**Kevin Smith**

HIGH-LEVEL LANGUAGES

French firm targets microcomputers with its version of Prolog

Grenoble, France—There has been no shortage of talk in the last few years about logic programming languages in general and Prolog, the language chosen by the Japanese for their fifth-generation computer project, in particular. But actual use of such languages is still largely limited to operators of certain mainframe computers.

But now a small French start-up company, Delphia S.A., thinks the time is ripe to make Prolog available to everyone who has a computer powerful enough to run the language. The firm has begun its quest by going to market with interpreters of its own D-Prolog (the D stands for Delphia) for three popular microcomputers. That the company's timing looks accurate is affirmed by support it has garnered from Hewlett-Packard (France) S.A.

"HP has given us a substantial amount of help, both in terms of equipment and personnel," points out Luc d'Arras, managing director of the firm, which is in Meylan, just outside this city. He adds that the Hewlett-Packard Co. subsidiary will put one of its HP9000 computers at Delphia's disposal some time this month to lend even more muscle to the smaller company's effort.

That the first real push to popularize Prolog should come from France is logical enough. The language was developed about 10 years ago at the University of Marseilles by a team led by Alain Colmerauer. One of Colmerauer's colleagues on that project was Philippe Donz, now d'Arras' partner at Delphia, who is the principal developer of D-Prolog.

D'Arras claims that Delphia's version of the language is considerably

Speed of treatment D-Prolog's claim to fame

With software houses new and old lining up to supply their proprietary versions of Prolog and other logic programming languages, for a given version to gain anything approaching broad acceptance will depend to large degree on its performance characteristics and ease of use.

For its D-Prolog, Delphia claims no less than the language's ability to resolve faster than any other language any problem that does not require a mathematical treatment. The company attributes this power to the fact that D-Prolog is not only every bit as flexible a language as the original Prolog, developed at the University of Marseilles, but incorporates a number of other features that further boost its performance characteristics. Several of these are particularly noteworthy:

- Since D-PROLOG includes the notion of a relational data base, it necessarily takes into account the relational model.
- It offers simultaneously systems for both interrogation and data manipulation.
- It makes possible the use of external programs written in evolved languages, thus enabling a user to take advantage of his library of existing programs. A program written in D-Prolog can operate in a Pascal, Fortran, or Basic environment, and vice versa.

The bottom line, according to executives at Delphia, is that a single instruction in D-Prolog is equal to approximately 10 instructions in a traditional language. This alone would be enough to justify the company's claim that its language makes it less expensive to realize a given application, whether or not a data base is utilized. The more that an application is "intelligent," the greater the saving becomes. –R.G.

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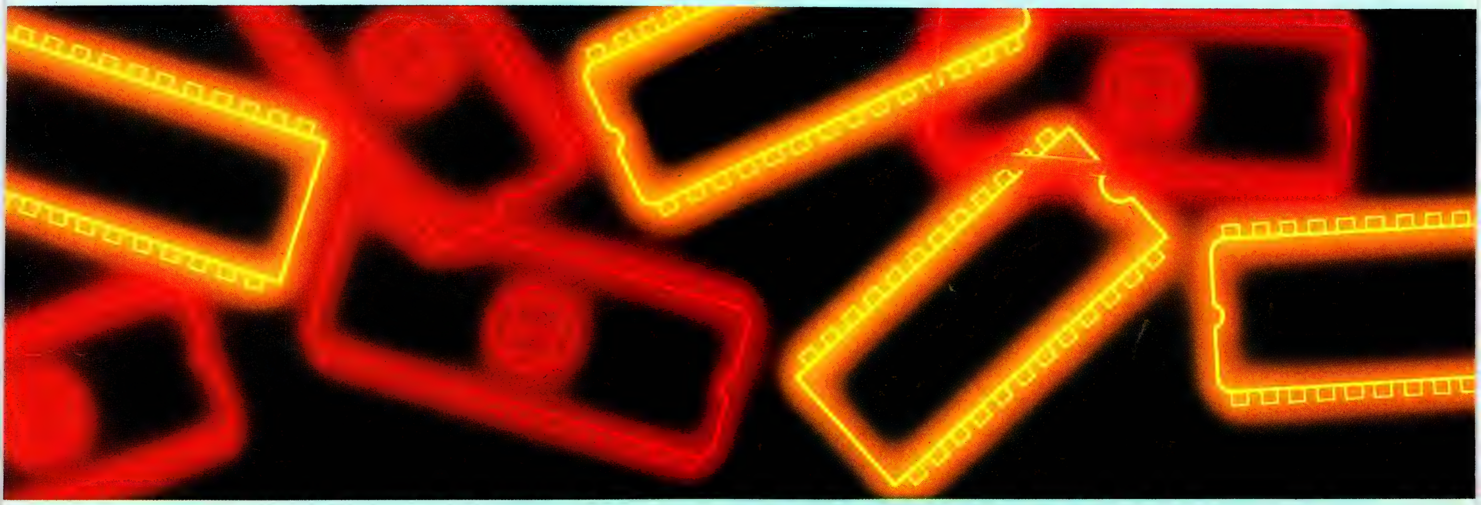

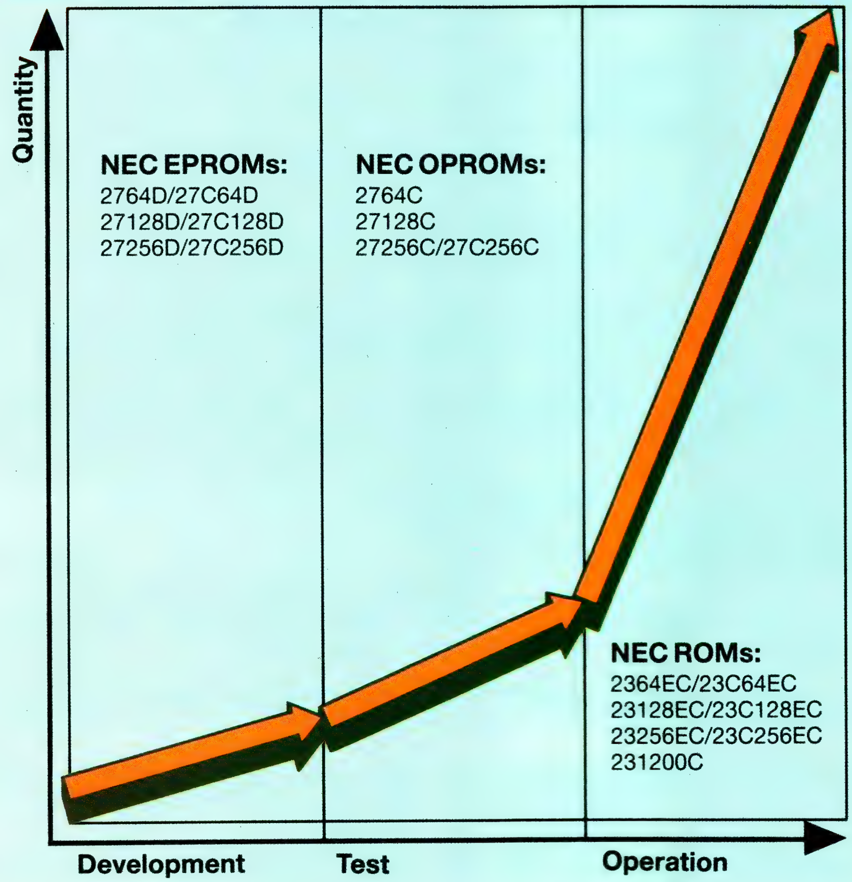

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more powerful than FOLL-Prolog (for First Order Logic Language), the most common existing version and available for use only on certain mainframe computers. D-Prolog exists already in versions for the HP 150, the IBM Personal Computer, and Victor-Sirius microcomputers. Interpreters for machines running 8086 MS-DOS and AT&T Bell Laboratories' Unix are in the works.

Others before. Delphia is not the first company to market a Prolog interpreter for microcomputers: there are already one or two versions of Prolog available for this class of machine, including a competing one on the market for the IBM PC. D'Arras asserts, however, that his company is the first whose objective is to make Prolog available on the broadest possible range of computers.

Usually, the language can be run on any 16-bit, or more powerful, machine with at least 512-K bytes of memory. Nonetheless, Delphia is considering bringing out an initiation version for computers that have half that memory capacity.

In addition to its hoped-for popularity in the microcomputer market, Delphia also expects to see Prolog play an important role in industry, particularly in the fields of artificial intelligence and computer-aided design and manufacturing. The snag is that the maximum performance for a Prolog interpreter on a microcomputer is in the area of 300 logical inferences per second, which is too slow for interactive control of industrial machinery.

To cash in on this market, the company is developing a D-Prolog compiler, which Delphia estimates would up that figure to several thousand logical inferences per second as well as permitting specific programs to be stocked on inexpensive read-only memories. D'Arras won't set a deadline for the compiler's completion, though he estimates the necessary development time at three man-years. **–Robert T. Gallagher**

CONSUMER

Upgraded analog monitor yields high-resolution picture

Tokyo—Analog technology got an unexpected new twist this week from Sony Corp. The Japanese consumer electronics giant is introducing a 13-in. multimedia monitor-type TV with variable horizontal and vertical scan frequencies for operation from virtually any picture source.

The monitor will go on sale in Japan on Oct. 21 and carry a price tag of about $510, the company says. It will be followed by a scan converter, tentatively priced at $815, that improves vertical resolution. The converter can serve as an enhancement for such products as video cassette recorders, video disk players, and home computers.

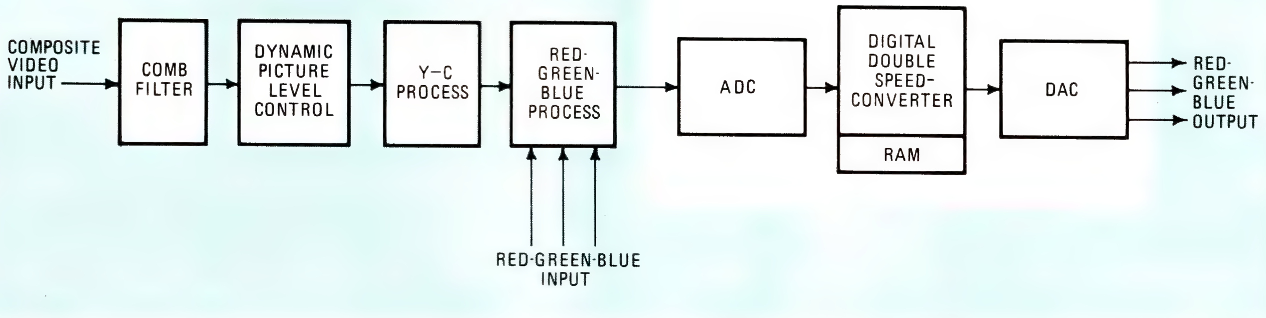
The converter uses Sony digital-TV integrated circuits similar to those used in the prototype digital receiver announced by the company last year [*Electronics*, Sept. 8, 1983, p. 77]. The comb filter, dynamic picture-level control, and luminance-chrominance processing circuits are analog, because the converter must have red-green-blue as well as composite video inputs. In considering cost versus benefit, Sony found it uneconomical to provide analog-to-digital conversion for both input types.

Captain videotex. Specific applications include broadcast TV at 15.75 kHz and the 31.5-kHz standard used by Nippon Telegraph & Telephone Public Corp.'s Captain videotex system, as well as converted noninterlace broadcast signals. Similarly, the vertical scan locks onto the incoming video signal over a frequency range extending from 47 to 65 Hz.

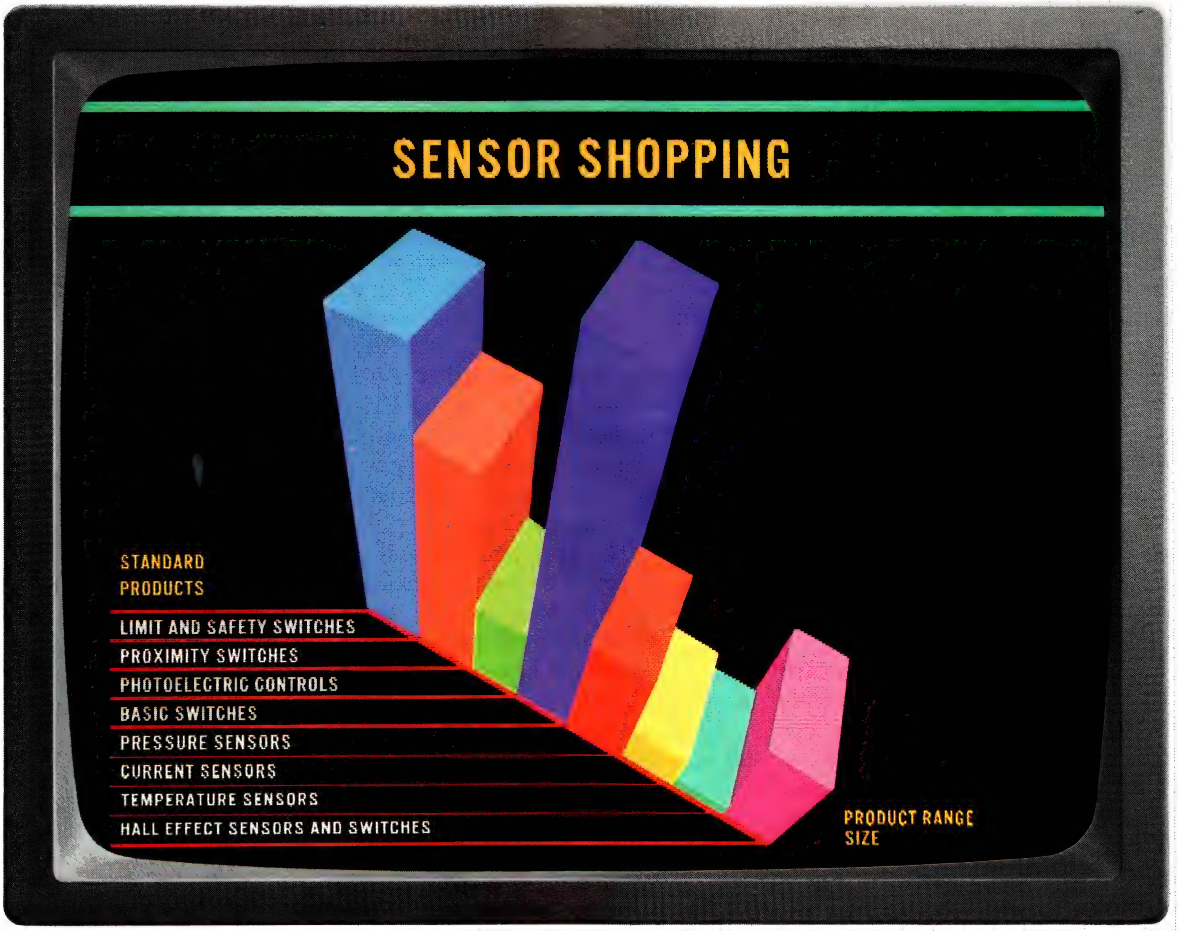
Masayuki Hongu, assistant general manager of Sony's TV Engineering Department and designer of the monitor, says that it extends the emphasis on high horizontal resolution started in Sony's Profeel line to the vertical direction. For TV reception, the monitor's horizontal resolution is on the order of 350 lines, with a composite video input resolution of about 450 lines and with an RGB input resolution exceeding 640 dots.

Horizontal resolution is enhanced with wide-bandwidth video circuits and fine-pitch picture tubes, which also enhance vertical resolution. The external noninterlace scan converter reduces interline flicker, thus improving the set's vertical resolution.

Right now, the set's main applica-



Analog and digital. The scan converter from Sony Corp. uses analog components to process composite video and red-green-blue inputs. The digital section interpolates scanning lines to provide noninterlaced scan for higher vertical resolution.



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tion would seem to be with broadcast TV and personal computers with RGB output, including a new breed designed to display 4,050 characters on monitors having a 55-Hz vertical scan and a 24-kHz horizontal scan. Sony engineers emphasize that the user can connect RGB or composite video signals for any of these functions, and the monitor will automatically display them properly.

True digital. Also scheduled for unveiling is a 25-in. digital TV with personal scheduling features, which marks Sony's debut into the nascent world of fully integrated digital television. It is tentatively priced at $1,380. Thus the firm becomes Japan's second manufacturer—after Matsushita Electric Industrial Co.—to announce its entry into Japan's digital-TV market.

The ICs for the receiver are supplied by Sony and ITT Intermetall GmbH, Freiburg, West Germany [*ElectronicsWeek,* Aug. 13, 1984, p. 49]. ITT Intermetall's chips are later versions of those used in Matsushita's set and use low-level digital signals and a low-level sine-wave clock to prevent interference from high-frequency broadcast signals. The set includes built-in digital processing for a telephone list, schedule list, electronic calendar with scheduling functions, and TV-program timer.

The scan converter will arrive in the U.S. in December. The 25-in. set will probably show up in the U.S. next spring, with the monitors and interlace scan converter to follow after that. **–Charles L. Cohen**

SECURITY SYSTEMS

Smart key does screening

Wetzikon, Switzerland—Melding old technology with new, lock-equipment maker Bauer Kaba AG has created an intelligent security system by integrating microprocessors and memories into what appear to be an ordinary door-mounted lock and key. The company expects the system, dubbed the Kaba Nova, to be used widely in hotels and office buildings.

Though Bauer Kaba is understandably cautious about revealing technical details, it says that the system basically consists of three parts: the key, a desktop programming unit, and an electronic unit installed in the door. The key is a reversible type—that is, its shaft has no specific top or bottom edge—pioneered by Bauer Kaba in 1934. A combination of dimples on the shaft matches the locking pins in the lock. The key's bow—the part of the key that is held to turn it—contains what Erich Seckinger, head of development at Bauer Kaba, describes as a very simple microprocessor and a nonvolatile memory for the user's code.

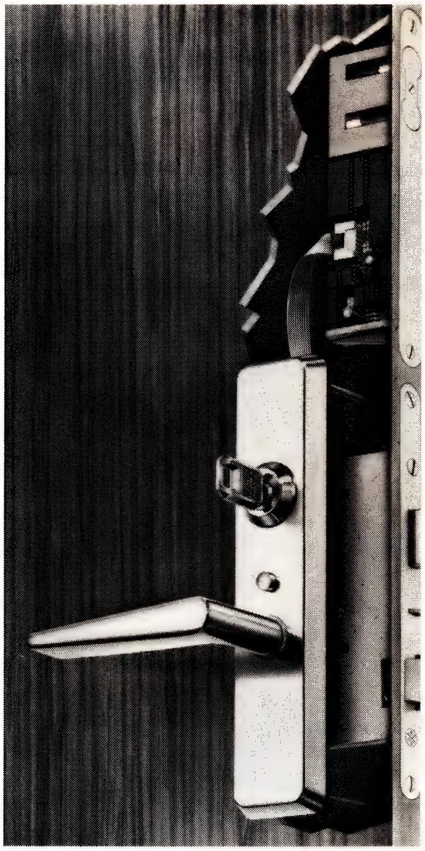
Coding. The programming unit encodes the key. To prevent unauthorized use, the programmer works only after the operator inserts his or her authorization key and enters a password on the unit's keyboard.

Next, the key to be coded is inserted into the programming unit. In a dialog carried out by a liquid-crystal display, the unit asks the operator for the visitor's name, his purpose, the rooms to which he will require access, and the level of authorization that should be granted. The operator punches out the answers on the keyboard, and these are then coded by the processing unit for storage in the key's memory chip.

This way, keys for a particular room or rooms can be custom-coded to allow one or several guests to enter, give one-time access to a repairman, or give full-time access to a hotel manager. Units can be configured to open doors only at certain hours or on certain days or, if connected to a data-processing system, provide an account of who entered a room and when.

The programming unit can also be used to erase a code or show which code an existing key contains. Each key has a precode imparted to it by the manufacturer, so that it can be used only in a particular hotel.

When the key is inserted into the lock and turned slightly, contact is made from the key's circuitry by way of its contact area to the electronic unit in the door (see photograph). The microprocessor in the key bow ensures that the code that is stored in the key's memory is properly transferred to the memory in the electronic unit, which must be programmed for that particular key.

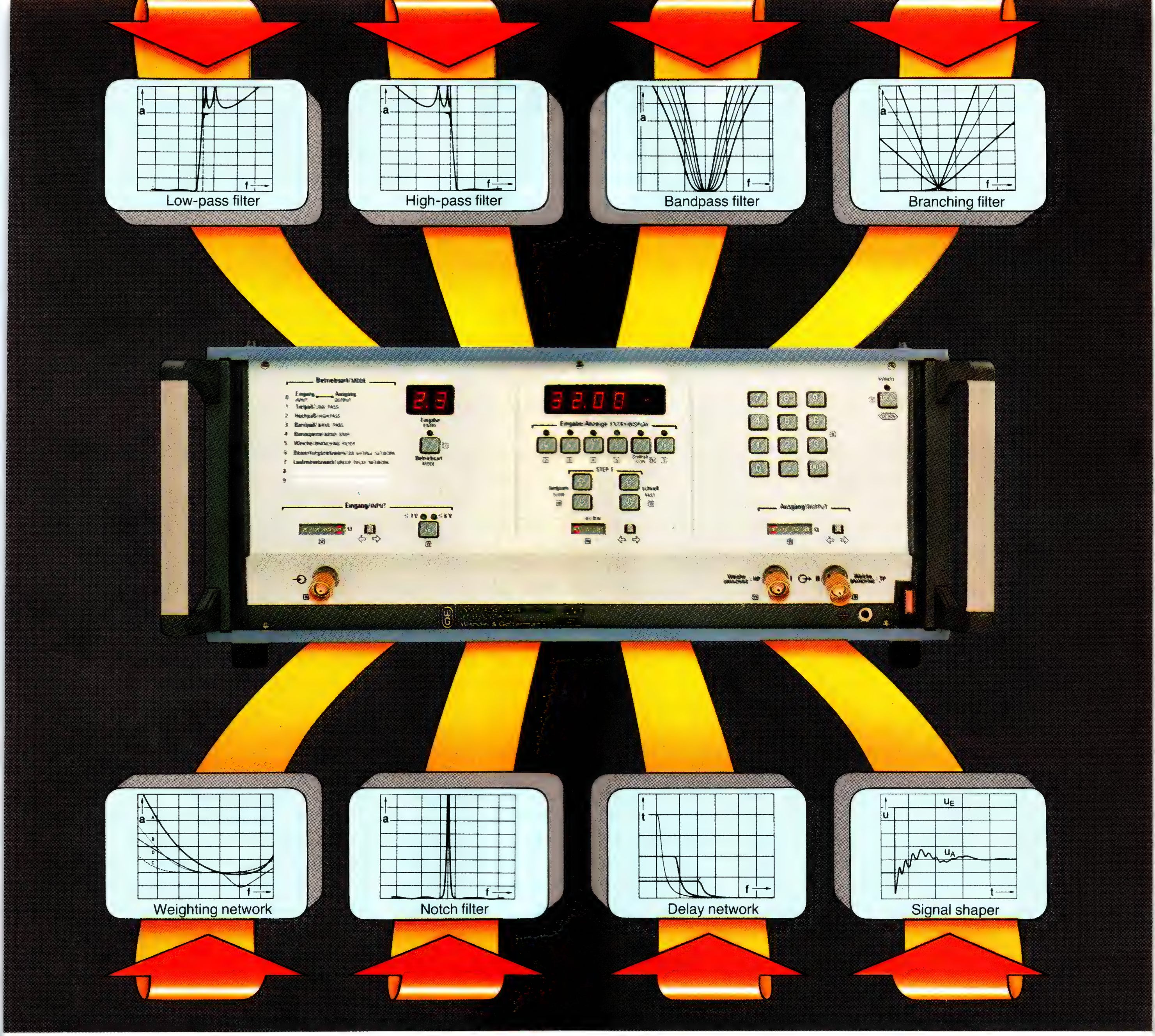


Muscle and memory. The Kaba Nova lock cylinder and electronic unit checks user authorization when the preprogrammed key is inserted into the cylinder and turned.

Only when the microprocessor-based circuitry in the door-mounted unit recognizes that the key code authorizes the user to enter the room can the user unlock the door. Powering the electronic unit are two 3-V lithium cells, enough for two or three years of operation. To save power, the system turns itself off automatically after unlocking a door.

Better than plastic. The Kaba Nova system has several benefits over systems using plastic cards containing codes in magnetic strips or punched holes, says Heinz Kuster, the firm's marketing director. For one, the key both mechanically opens the door and carries the code that authorizes the user to enter a room, making for one-hand operation. In addition, plastic cards, especially those with a hole code, can easily be copied. Not so the new system's code, as it can be read out only with specialized electronic equipment.

Further, unlike most card systems, Kaba's can easily be integrated into a multitude of lock constructions. Ac-



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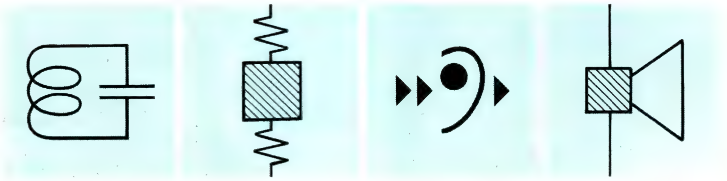

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cording to Kuster, the programming unit will be priced at roughly $2,000, the electronic door unit at about $280, and a key with its microelectronic circuitry at $10. **–John Gosch**

INDUSTRIAL

Modules aid interfacing

Freeport, Ill.—Sensing devices are essential to the automation of factory processes, but the job of hooking them up to current-generation programmable controllers or host computers can be time-consuming and costly. A solution, however, may be in the offing from the Micro Switch Division of Honeywell Inc.

Last month, the company began shipping a product called the SID-2000 (SID stands for sensor interface device) that is designed to bundle into one box all the interface functions for a wide variety of sensors and manual control equipment. Instead of relying on the user to wire up his own sensor interface, the SID-2000 puts the necessary signal-conditioning circuitry for various types of devices into modules. Each module can then be added to the system according to the sensor types needed for the application.

Input modules for fiber optics, analog sensors, and a variety of ac and dc sensors are among those initially offered, including one that contains a built-in dc power supply. Once put into necessary form, the sensor input data can then be passed along to a programmable controller or host computer for further manipulation or process control. Because the SID unit includes its own Z8-based single-chip microcomputer (with common functions such as timers, counters, and shift registers), it can also be used in a stand-alone mode.

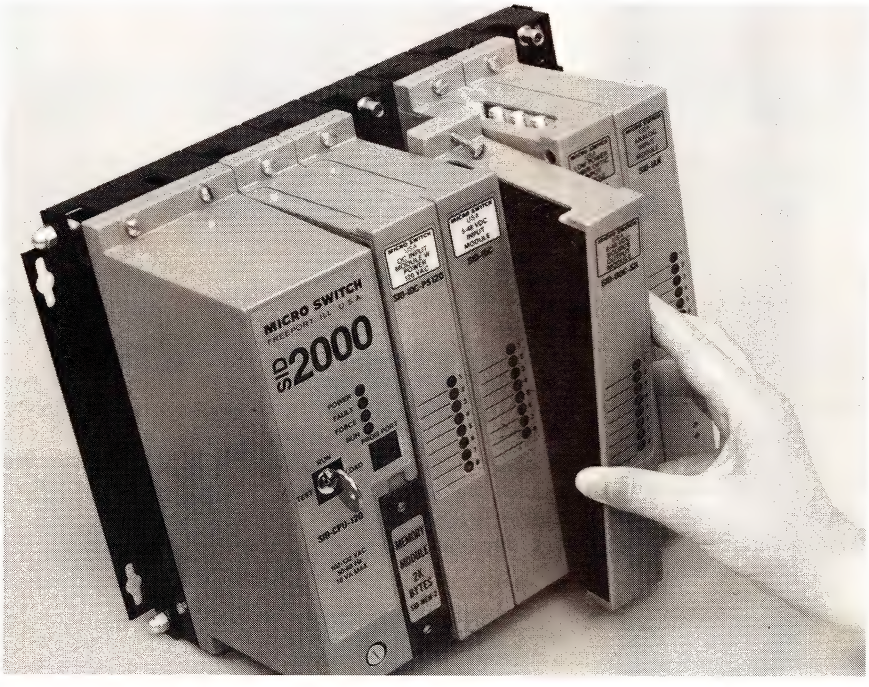
Several SID-2000 output modules are available for driving various types of equipment. The Micro Switch system provides for either 2-K bytes or 8-K bytes of user program, housed in electrically erasable programmable read-only memory. A portable, battery-powered programming unit with a 33-key touch panel, a liquid-crystal display, and its own Z8 microprocessor is also provided for program development.

In all, the SID-2000 can be configured for a maximum of 160 input/outputs, at eight channels per module. Depending on the type, modules are priced between $130 and $450 each. Typical systems requiring three or four modules will sell for about $1,500, including the central processing unit and programmer, says Richard L. Rowe, Micro Switch new product design manager.

Because of its built-in logic capability, the SID unit is likely to compete in the market against low-end programmable controllers built by Gould Inc., Allen-Bradley Co., and others. In fact, the Micro Switch system will provide more I/O and analog channel-handling capability than most programmable controllers in the same price range, according to William Bright, senior outside sales engineer at Steven Engineering Inc., a South San Francisco industrial control distributor.

The limit. "We tried to put in everything that a small programmable controller can do on the logic side," says Rowe of Micro Switch. But he stresses that the division has no plans to push into the programmable-controller business. "We are not going to get any more expensive or larger than this," he contends, adding that the SID-2000 will be a major benefit to Micro Switch's sensor business. The SID-2000 will also work with many sensors supplied by other manufacturers.

As a broad-line supplier of sensors and manual controls, Micro Switch sells equipment for sensing position, pressure, current, temperature, and airflow, and is working on detectors for velocity, vibration, and other parameters. By providing SID modules for use with each new sensor type, Micro Switch hopes to simplify the user's automation task and cut down on the time its own engineers must spend helping customers interface its sensors. **–Wesley R. Iversen**

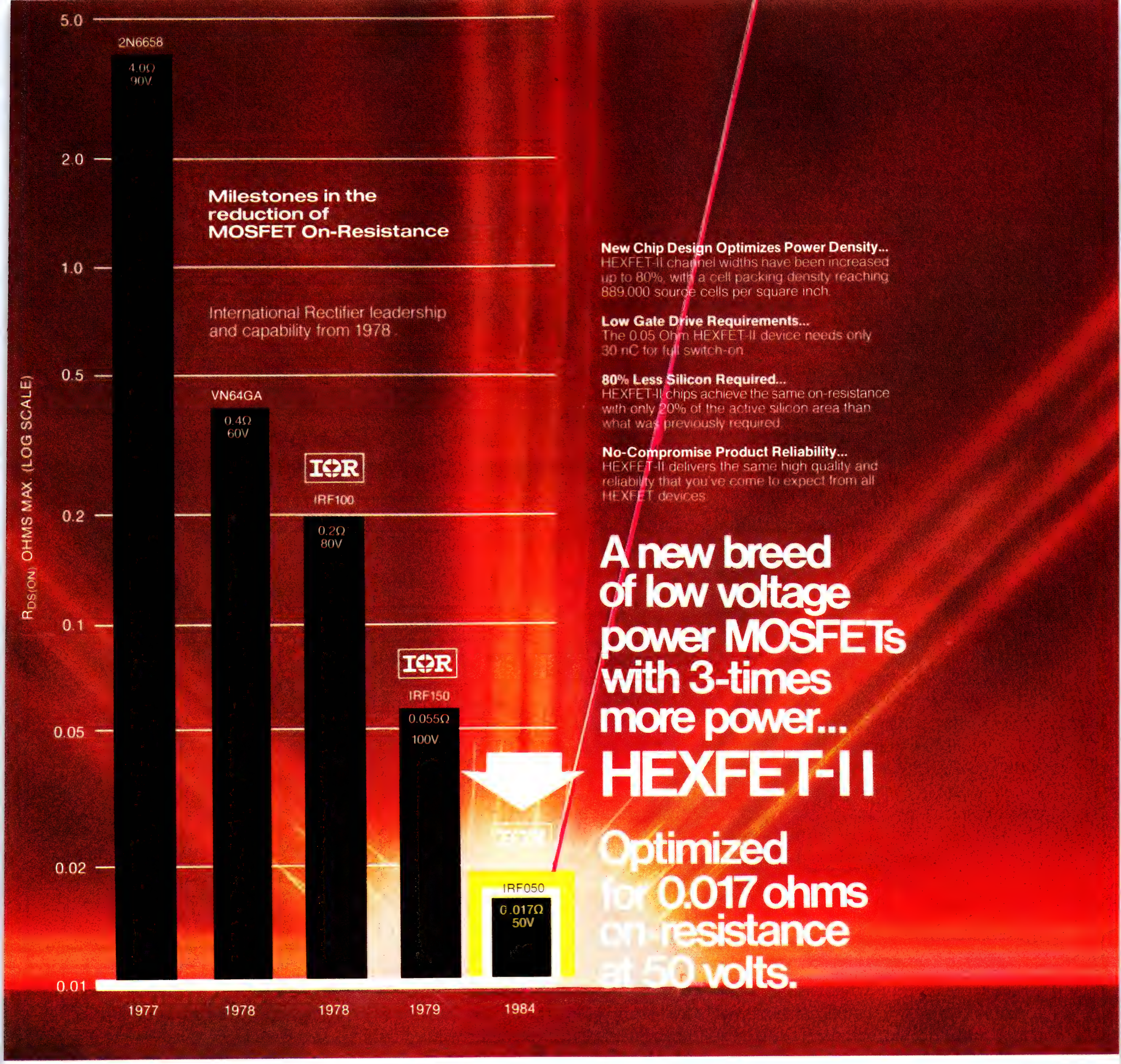


Handy way to customize. Input/output modules plugged into a backplane that also carries the sensor interface package (left) match the SID 2000 system to the application.

PRINTED CIRCUITS

Dye spots pc-board flaws

San Diego—With the aid of a new process that ferrets out defects in printed-circuit boards, the Air Force expects a large payoff for a small investment: the saving of some $2 million over a five-year period for an initial outlay of $163,700 to develop



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the technique and another $334,000 to exploit it. If the other military services come on board, savings will climb into the tens of millions of dollars. And widespread commercial adoption could send that figure soaring even higher.

Developed by Science Applications International Corp. here, the technique is relatively simple by high-technology standards. It calls for spraying a solid dye sheathed in polymeric capsules of 1 to 10 micrometers in size onto pc boards as they move along a carousel-like conveyor system. The dye lodges in mechanical and structural imperfections in the boards and causes them to flouresce under ultraviolet light. A closed-circuit TV system with a charge-coupled-device camera displays the defects on a 19-in. screen.

Encapsulation of the dye is like "enclosing each particle of dye in a miniature beach ball and then shooting them at the crack or fault," explains 1st Lt. Ernest J. Mueller of the Air Force's Aeronautical Systems Division at Wright-Patterson Air Force Base, Dayton, Ohio. "The beachballs wedge in tightly and actually project over the rim of the crack, making it much easier to see them during inspection."

The dye itself, supplied by Magnaflux Corp., Chicago, has the consistency of a powder and tends to explode against the surface of the board, resulting in extremely small particles that do not stick in sufficient quantity to be easily detected. Liquid penetrant, which is used for many inspection applications, was tried but rejected because it corrodes or soaks into the fiberglass used for the boards, he adds.

Slow job. Currently, Air Force quality-assurance inspectors use microscopes to study problem boards, explains Mueller. With the increased packaging density of electronic components and narrower conductive lead paths, troubleshooting to detect faults is becoming an extremely time-consuming and expensive job. It now takes up to six hours to examine one board and the probability of error with the microscopic procedure is quite high because each inspector has to rely on his own experience and judgment. With the Science Applications process, inspection time should drop to one minute per board.

Still in laboratory development, a prototype unit will go into operation at the Ogden Air Logistics Center, Hill Air Force Base, Utah, in early 1985. After a successful test trial, the system will also be installed at Warner Robins AFB, Ga. Both these facilities handle about 60% of Air Force repairs, amounting to 50,000 boards per year.

If all goes well, Mueller expects that all the services will buy the Science Applications system. Reducing the time and costs of board inspection is a high priority. With the aging of military products, the inventory of faulty boards goes up. "The services have no other alternative than to repair them because replacements are simply not available anymore," he points out.

Primarily a research and development firm serving the military, Science Applications has not given much thought to marketing its process to commercial end users. But as the firm gets calls from the likes of Gould Inc., management is starting to pay heed to sales opportunities in the private sector. **–Karen Berney**

DYNAMIC MEMORIES

Thomson enters DRAM business with boost from Oki and IBM

Paris—The semiconductor division of Thomson-CSF will hit the ground running when it enters the dynamic random-access memory business before the end of the year. Two separate contracts will simultaneously provide technical support for the industrialization of the DRAM integrated circuits as well as provide a major customer to get their commercialization off at speed.

According to Jacques Noels, director of Thomson-CSF's components branch, the French company will be using its own technology but get substantial production assistance from a five-year industrial know-how exchange recently signed with Oki Electric Industry Co., of Japan. The agreement covers both memories and gate arrays.

The probability of financial success is strengthened following a huge order placed by the IBM (France) subsidiary of IBM Corp. for more than $100 million worth of the DRAMs over the next three years. For IBM, the deal has a double attraction.

First, it gives the U.S. company a second European source for memories, after Siemens, at a price that is fixed into the future. In addition, IBM is seen as supporting the European electronics industry at a time when its own role in the European market has been put into question by the European Communities [*ElectronicsWeek,* August 13, 1984, p. 20].

Memory maker. Jacques Noels has moved Thomson-CSF into the DRAM business as part of his bid to propel the French firm into the top ten semiconductor houses by 1990.

Thomson's entry point into the memory market will be the 64-K RAM, a part that Noels says the company has been producing regularly over the last year in pilot quantities. The company's 64-K RAM has already been qualified by IBM's European supply center in Bordeaux. Thomson, which trades in ICs and discreet components under the name of Thomson Semiconducteurs, expects to begin shipping samples of a 256-K RAM by the middle of next year. It projects that it will have production of the chip in full swing by

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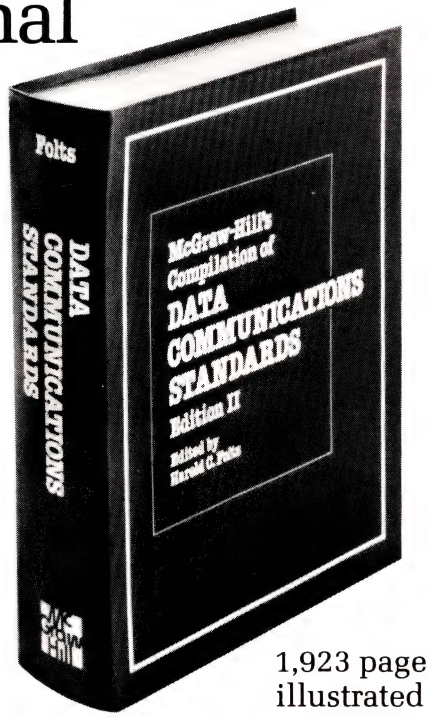

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no later than the end of the year.

Noels considers Thomson's participation in the DRAM market central to its overall objective of commanding 3% of the world market and being among the top 10 semiconductor houses by the end of this decade [*ElectronicsWeek,* July 30, 1984, p. 45]. Though he admits that MOS memory is a risky business, Noels feels that the kind of volume that such products generate is essential to reducing fixed costs and thus making a manufacturer more competitive over the entire range of his product portfolio.

Most industry observers were surprised that Thomson chose a Japanese partner after its five-year-long collaboration with Motorola Inc., which included technological transfer. Noels explains that while Motorola was willing to agree to a product transfer, Oki gave a more positive response to Thomson's desire to participate in a broader pact aimed at mutual industrialization of memories. The two companies will jointly produce and market their existing respective lines of gate arrays and will rationalize related software.

The Thomson-Oki deal follows on the heels of two others announced last week. The first distinguished Thomson as the first company to acquire second source rights to the Motorola 68020 32-bit microprocessor. The other, a reciprocal second source agreement in the consumer IC field with Telefunken Electronic GmbH, Heilbronn, West Germany, puts both companies in the thick of the battle to supply chip sets to equipment manufacturers that will be producing the next generation of highly integrated TV sets.–**Robert T. Gallagher**

INTEGRATED CIRCUITS

New system could pave the way for simplifying IC designs

Los Gatos, Calif.—A new integrated-circuit design system brought out last week by Silicon Compilers Inc. could prove to be the long-awaited tool that greatly simplifies the development of very large-scale ICs. Using the new product, a systems designer who lacks the proficiency of a master IC craftsman can style chips with a functional quality that nearly approaches custom design, yet with a much shorter design cycle.

The methodology used by the new Genesil Silicon Development System is silicon compilation, a process that takes high-level architectural instructions and synthesizes complex designs for a silicon foundry [*Electronics,* May 3, 1984, p. 121]. Genesil is a turnkey system consisting of a Digital Equipment Corp. VAX 11/750 computer with 4 megabytes of main memory, a disk storage system with a 450-megabyte capacity, tape storage, and four high-resolution color work stations. System software provides for IC definition, functional simulation, timing analysis, place and route, testout, and tapeout.

Genesil is more than the next step in the evolution of engineering tools, such as those for computer-aided design, and more flexible than the current proliferation of standard-cell libraries for semicustom design, according to the company. The system marks a departure from the standard approach to VLSI design. Walter P. Curtis III, Silicon Compilers' marketing vice president, believes the opportunity is right for a revolution in design tools. "The business is at a stage where you're using any tool you can get your hands on."

Big growth. Citing statistics put out by market research firm Dataquest Inc., San Jose, Calif., Curtis points out that by 1990, one quarter of all systems engineers—or a total of approximately 100,000—could be designing their own circuits. This growth "can't be sustained by existing design tools that are in the marketplace."

Aimed at computer systems designers, military contractors, and semiconductor houses, the system will initially be available with an n-MOS function set; a CMOS function set will be ready in the first quarter of 1984. The system's base cost—$545,000—and the cost of maintenance on the system (charged at the monthly rate of 1.2% of the original selling price) represents a heavy investment, which has to be weighed against several benefits.

Time is money. According to Mary Wu, an analyst with market research firm Gnostic Concepts Inc., San Mateo, Calif., a chip design firm's selection of design automation tools and services "boils down to how much a company wants to pay for the turnaround time." In terms of time, Curtis believes Genesil has everyone beat. The process has been used for three merchant chips, including the processor for DEC's MicroVAX I, which had a design cycle of only seven months [*Electronics,* Oct. 20, 1983, p. 47].

Born out of research at the California Institute of Technology by David L. Johannsen (under the guidance of Carver Mead), the tool's toughest challenge to-date has been industry acceptance that the concept is not overly research-oriented and that it does not sacrifice silicon efficiency. A comparison of the MicroVAX 1's silicon efficiency statistics versus those of Intel Corp.'s 80286 processor shows that routing on the MicroVAX 1 consumes only 13% more area.

Aiding the front-end architectural freedom is the system's short instruction period and quick compilation, which builds a model up at the average rate of 30 transistors a second. With such speed, notes Curtis, "you can go through that [design] loop several times a day." The firm also says the flexibility brought about by the inclusion of as many as a dozen silicon foundries' parameters will offset any inherent loss of silicon efficiency as compared to design methods that lock the designer in to one foundry early in the process.

Critical of the current design tools, Curtis says that gate arrays are not a good long term solution. Furthermore, he says, "anything you can do with a standard cell, I can do with a silicon compiler, and probably better."

Silicon Compilers expects to ship four to six of the systems this month to beta test sites. –**Eve Bennett**

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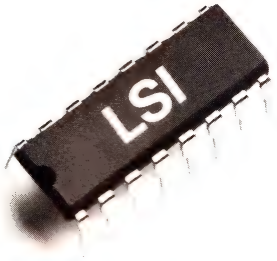

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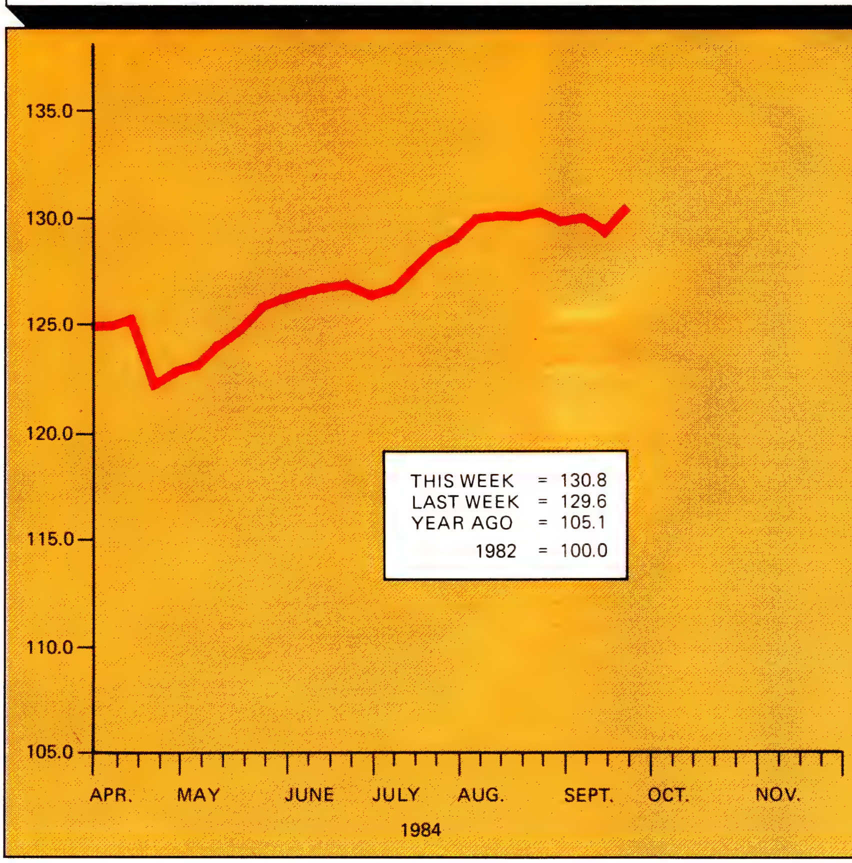
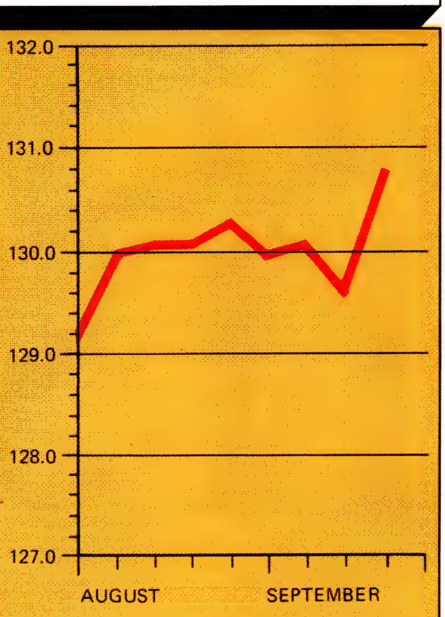
ElectronicsWeek Index



THIS WEEK = 130.8
LAST WEEK = 129.6
YEAR AGO = 105.1
1982 = 100.0



The *ElectronicsWeek* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear below from week to week.

U.S. INDUSTRIAL PRODUCTION AND COMPONENTS PRODUCER PRICE INDEXES

	July 1984	June 1984	July 1983
Office and data processing equipment	325.4	322.2	267.5
Communications equipment	212.2	204.0	184.4
Radio and TV equipment	130.1	111.1	110.8
Electronic and electrical instruments	177.3 (August 1984)	175.9 (July 1984)	161.6 (August 1983)
Components	465.0	443.4	368.4
	August 1984	July 1984	August 1983
Digital bipolar integrated circuits	62.8	63.1	64.2
Digital MOS ICs	42.3	42.9	40.6
Linear ICs	65.3	65.8	63.3
Capacitors	191.9	190.6	192.9
Resistors	184.5	185.1	184.0
Relays	319.3	319.1	301.2
Connectors	229.1	228.8	223.6

An increase in production for all segments of the electronics industry helped the *ElectronicsWeek* Index move up in the latest reporting week. The largest gain was in production of radio and television equipment, which rose 17% in July. In spite of heavy penetration by imports, July's production level for radio and TV systems is the highest in 30 years. In part, this is due to foreign firms moving some of their operations to the U.S. In other segments, production of communication equipment and components was up 40%.

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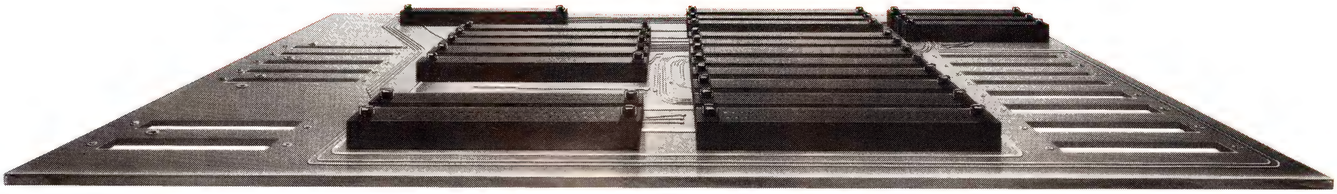

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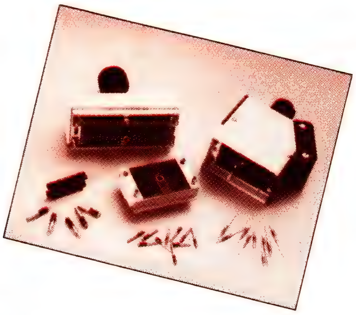

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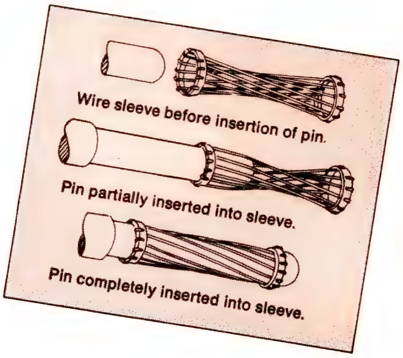
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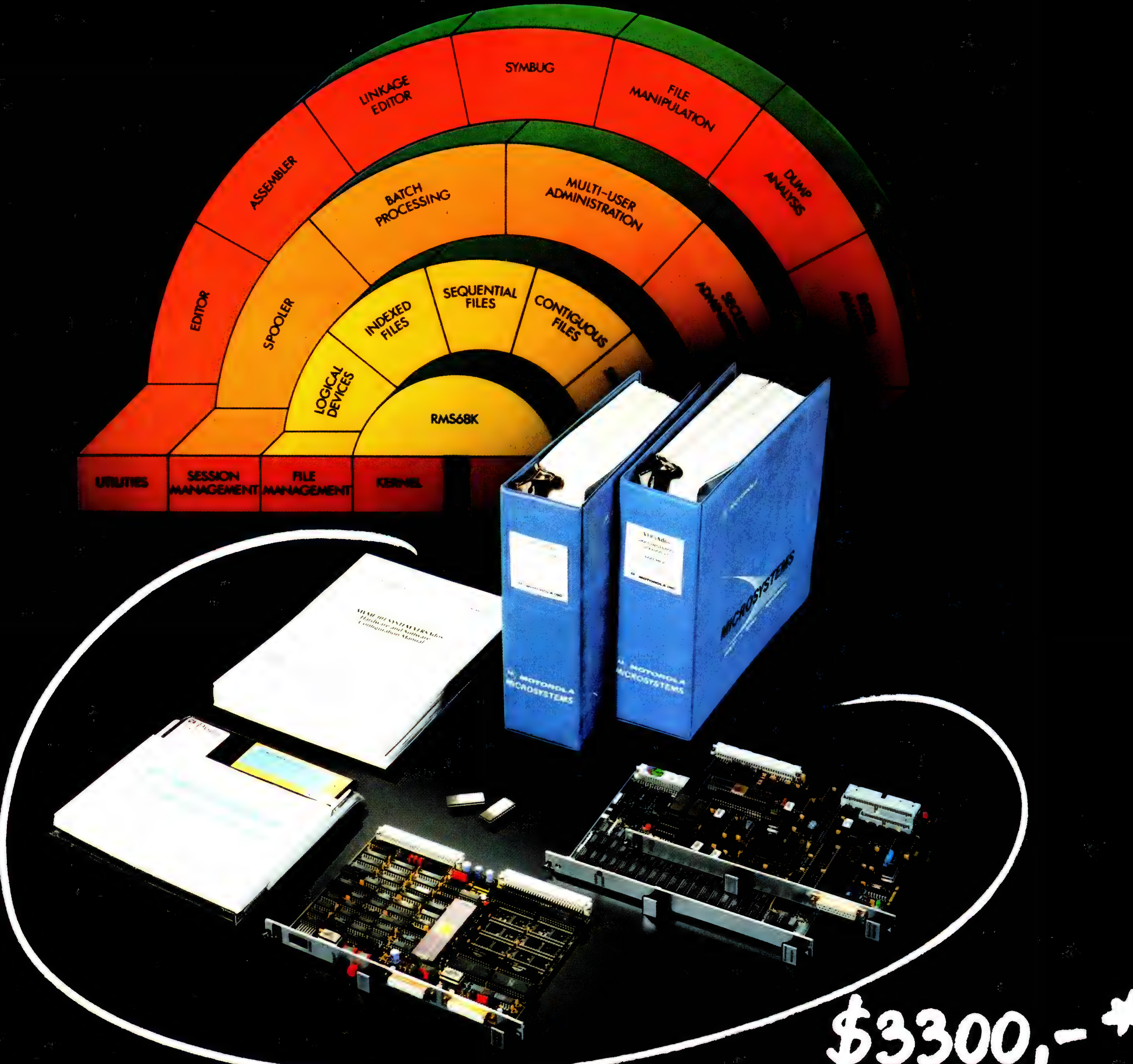

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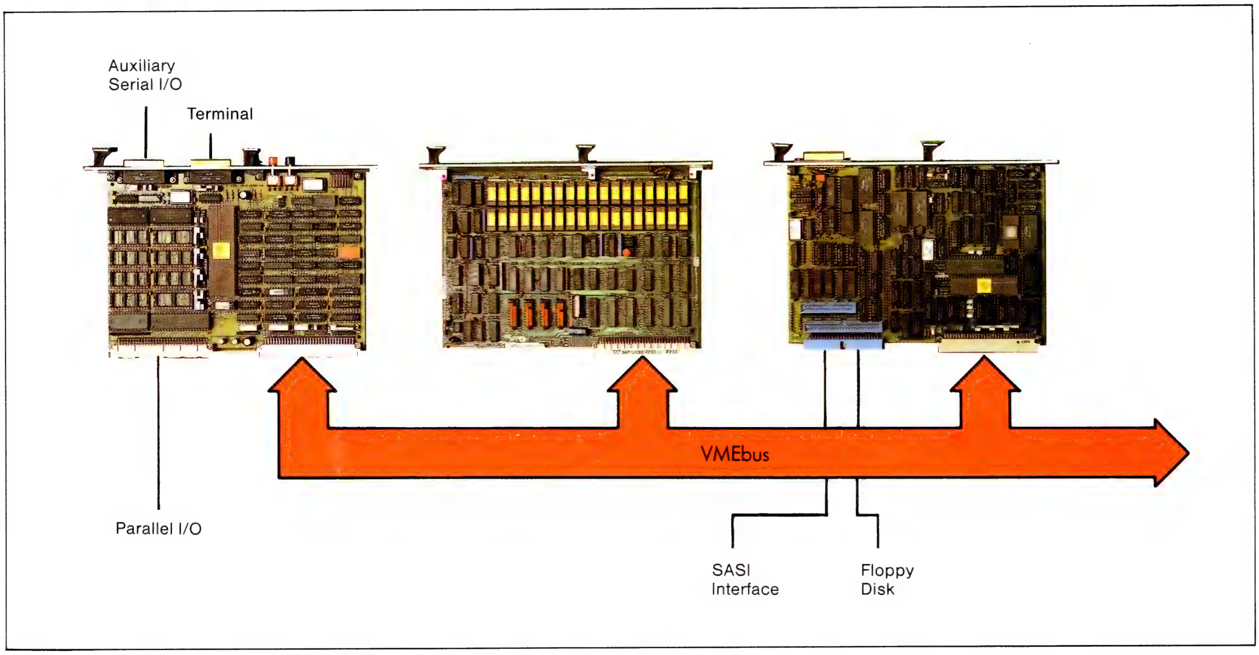

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BOMBA MIXES TECHNOLOGIES IN INDUSTRIAL APPLICATIONS

Milwaukee, Wisconsin

"I started out to be an electrical engineer," says Steven J. Bomba, "but I found out that I was so interested in the whys and wherefores, that math and physics appealed to me more." Thus it is not surprising that the 47-year-old Bomba is the holder of BS, MS, and Ph D degrees in physics from the University of Wisconsin. Nor is it unusual that the man who says he enjoys classical physics and "the application of physics to the world around us" should be heading up industrial research efforts for Allen-Bradley Co.

When you think about it, says Bomba, the job of industrial control research is largely a matter of picking out leading-edge technologies employed in other fields such as defense, or consumer electronics, and figuring out how they can be advantageously applied in the factory. Bomba calls the process "technological synthesis." And he can point to at least a couple of promising technologies out there now that are ripe for industrial application.

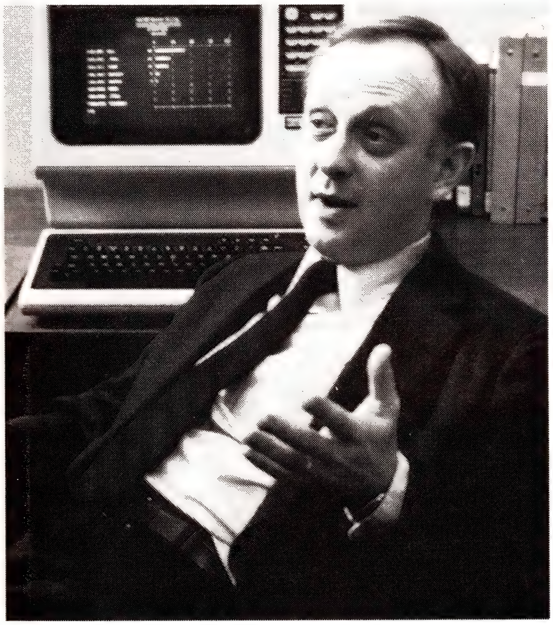
One is the digital audio disk. "Audio is typically reproduction of sounds up to 20,000 hertz, and if you look at factory processes, you'll find that the usual frequencies of change you see are on the order of thousands of hertz at most, which means they fit neatly into that technology." Potential applications are numerous. For example, the auditory signature of any number of typical machine ailments could be stored on disk. "Then," Bomba explains, "you could place a mike on a machine and compare what you hear to known sounds and you'd know you'd better replace bearing number 12."

Another technology that Bomba predicts is likely one day "to cause a revolution in communications for the factory, the likes of which nobody today can even think about" is free-space optical communication. IBM researchers in Zurich, among others, have been working on the concept.

He notes that the idea, which involves placing a photodetector and transmitter in the ceiling for communicating with any number of similarly equipped machines in a room, has always looked good. But, Bomba believes, recent breakthroughs in the technique of optical heterodyning may now be bringing free-space communication much closer to reality.

Bomba, who grew up a ham radio operator and electronics hobbyist, has plenty of work experience to draw upon. Before joining Allen-Bradley in 1978 as director of corporate technology development, his career included stints with Mobil Research and Development Corp., where he worked in applying computer and communications technology to the oil field; Texas Instruments' corporate research laboratories, where he helped develop proprietary consumer products; and Rockwell Collins Radio, where he dealt with satellite communications.

While Bomba is confident that DAD and free-space optical communication will one day find their way into the factory, he is making no predictions as to when. Such advances have a way of taking longer than expected, he says. "Look at fiber optics. It reduces cost and it improves performance. Down in the lab, we do all kinds of wonderful things with it. We sense with it. We communicate with it. And we wonder why people still aren't using it in the factory." **–Wesley Iversen**



Synthesizer. Steven J. Bomba sees his job as largely a matter of picking out leading-edge technologies and deciding how to use them in the factory.

Sakamura's operating system leads the way for Japanese advances in computer science

Tokyo

Now that microprocessors are powerful enough to support operating systems that use Japanese language processing facilities, Ken Sakamura is convinced that Japanese computer scientists will find it easier to make important contributions. The 33-year-old assistant professor at Tokyo University's Department of Information Science is in fact leading the way—he is the first to develop a microprocessor operating system adopted by a major manufacturer, NEC Corp.

NEC is only the first to announce a product, though. Sakamura says that he is also working with four or five other firms. "I would be equally happy to work with American or

Successful. Ken Sakamura developed a microprocessor operating system adopted by a major company, a Japanese first.

other overseas firms too," he says.

Actually Sakamura's operating system is only one part of a clean, new architecture for very large-scale integrated circuit real-time microprocessors that will have the operating system nucleus incorporated in silicon on the chip. He calls the architecture Tron, for The Real-time Operating-system Nucleus.

It will be available in three versions, he says—industrial, business, and home—with an applications software bus for exchanging data among the variations. Software versions will be used to develop both applications and training programs for applications implementers in the period before silicon chips are available.

Sakamura says that all-new designs are needed because present microcomputers have untidy architectures that grew out of 4- and 8-bit chips developed when IC technology was limited. He thinks that CP/M accomplishes quite a bit for the small amount of memory that it uses, but that it is too limited for modern applications. Intel's real-time operating system cannot be used for business applications, he says, because its file structures are inefficient.

Sakamura's present work on operating systems grew naturally from his graduate studies. For his dissertation, he developed a computer architecture in which the microprogram changes adaptively with the program being run to dynamically vary the computer instruction set. Thus, the computer is provided with a learning function that makes for an increase in speed with repeated passes of the same problem. He gave a paper on his work at the National Computer Conference in New York in 1979.

In addition to his position at Tokyo University, Sakamura is an instructor in computer science at Keio University in Yokohama. He thinks computers are fun to play with even when he isn't working, and he is proficient in a large number of languages. **–Charles L. Cohen**

Business is a tough game, but Automatix's new president is in it to win

Billerica, Mass.

One of the best things that happened to Michael Cronin since he became president of Automatix Inc. in June was the signing of a letter of intent to enter into a relationship with General Motors Corp. That agreement calls for GM to buy 10% of the company's outstanding shares and to fund research and application efforts. Not bad, by any standard.

Soon after that letter was signed, however, Automatix, which is in the robotic and machine vision businesses, lost a major order from GM to a competitor. So right away Cronin found out that the relationship with GM was not a guarantee of the profitability that has thus far eluded the four-year-old company.

Cronin moved up from vice-president of marketing to succeed Philippe Villers, Automatix's president since its founding in 1980. "The company had gone through the entrepreneurial phase, and the feeling was that we should change the tone of the corporation from an entrepreneurial one to a profitable one," he says.

Cronin received his electrical engineering degree from Boston's Northeastern University in 1961 and his MBA from Harvard in 1963. After two years in the army, he worked in marketing for what was then called Baird Atomic (now just Baird Corp.), before leaving to launch his own minicomputer company.

After bombing with the start-up, Cronin did the only logical thing: He worked as a consultant, telling other people how to run their businesses. One client was ComputerVision, who took his recommendations seriously enough to hire him as marketing manager and eventually promoted him finally to executive vice president in charge of hardware and software development. ComputerVision became an industry success story and by the time he was 40, Cronin says he was financially secure and ready for his next career move.

Head coach. Michael Cronin's job will be changing Automatix from an entrepreneurial company to a profit-oriented one.

Enter Automatix, Inc. In only four years, the company has already achieved a leadership position in the industrial vision business and an enviable relationship with GM. What Automatix has not done to this point is show a profit. This is what Cronin says is his top priority.

Already there have been changes. For one thing, Cronin no longer wants the company referred to as an industrial robotics and machine vision company: "We are the adaptive automation company." Cronin also intends to direct the company's engineers into developing more profitable products for marketing into higher volume areas. **–Craig Rose**

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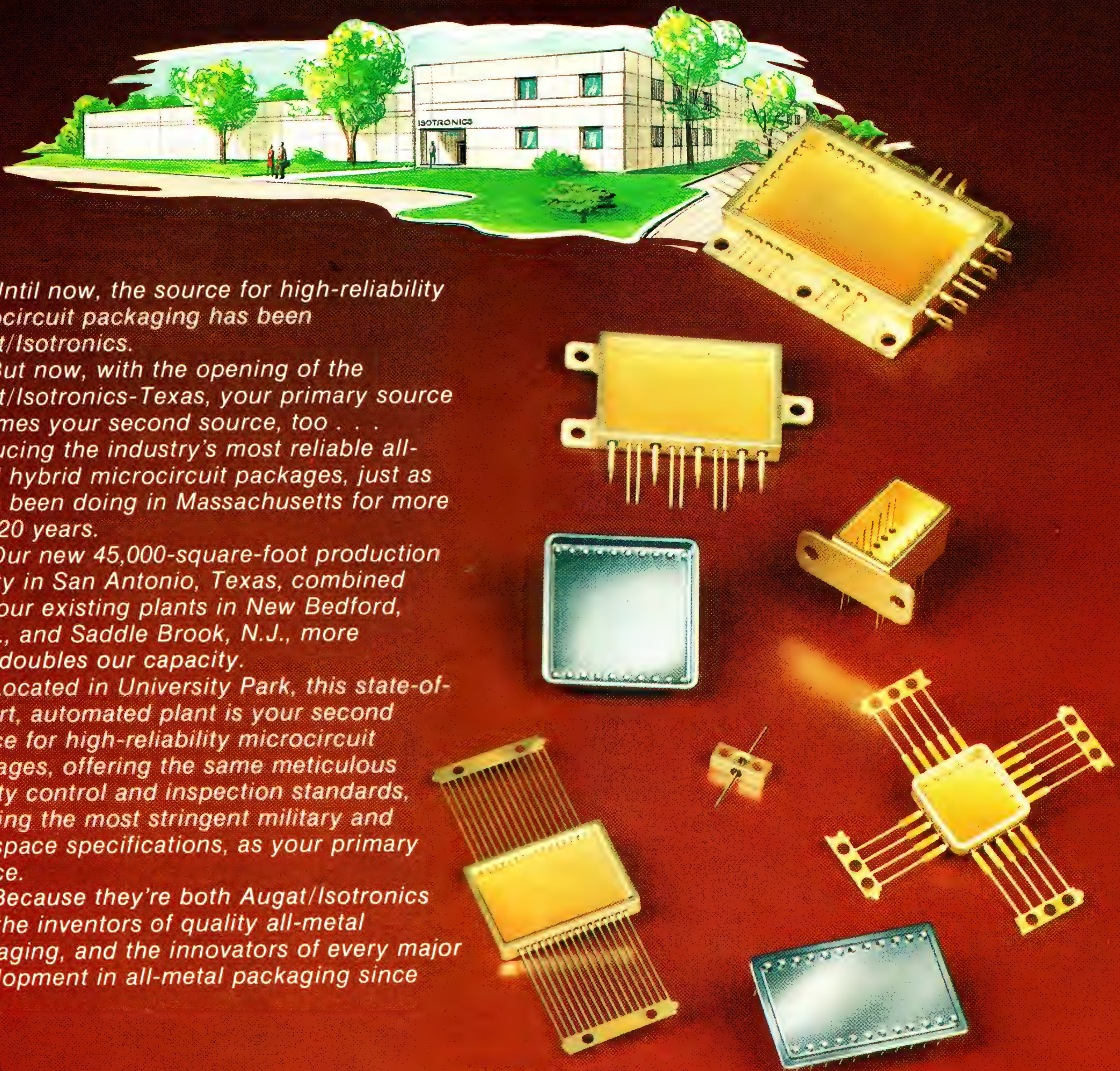

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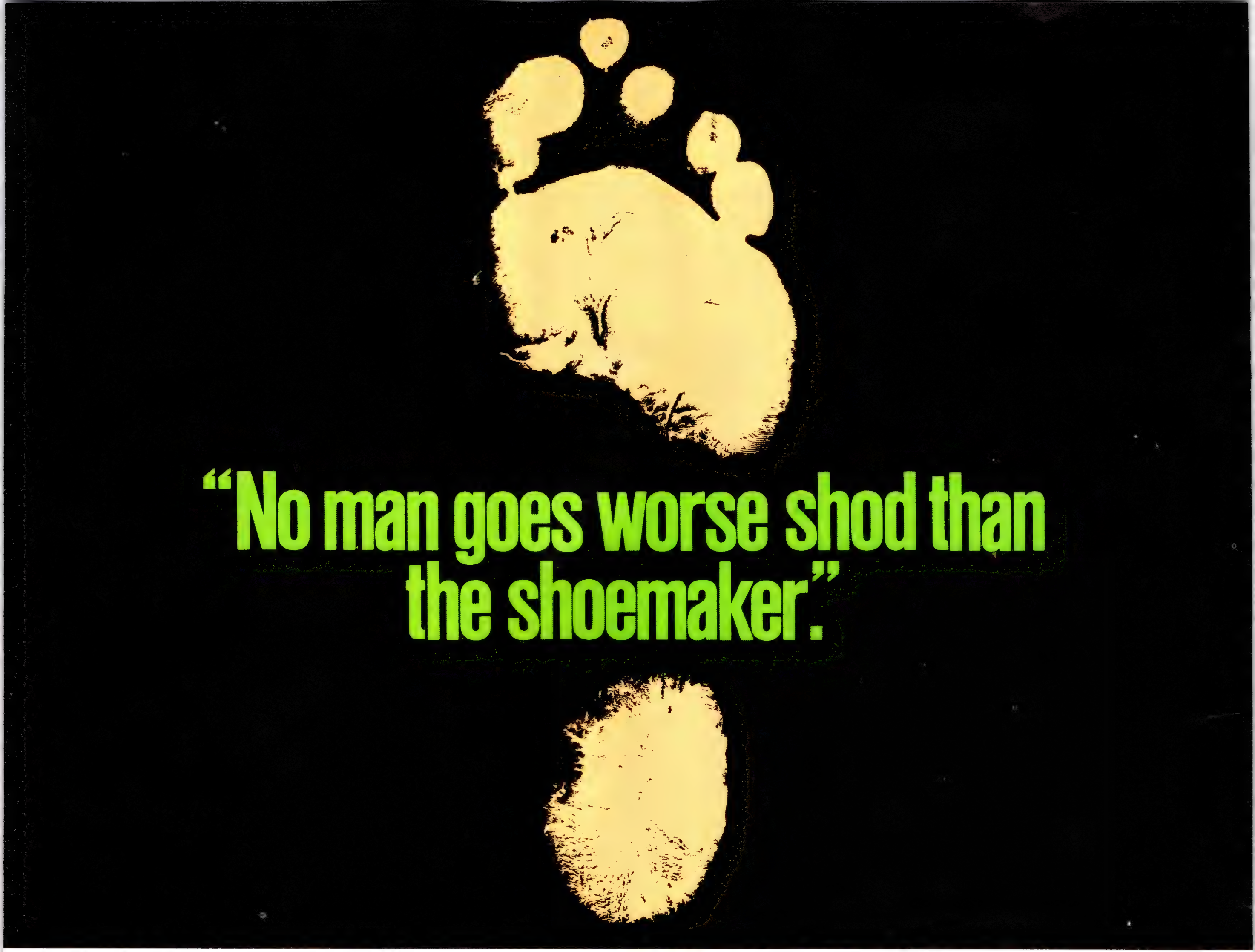
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KODAK TURNS MANUFACTURING EXPERTISE TO ELECTRONICS

Rochester, N.Y.

The company that brought inexpensive mass-produced cameras to the U.S. public 40 years ago is now turning some of that expertise to the electronics market. Eastman Kodak Co.'s U.S. Apparatus Division here has 6.1 million ft^2 of space, where electronics technology abounds and in which it plans to make a range of equipment for the information-processing industry.

Kodak has already brought out its first entry in the electronics market. Under a second-source agreement, it is producing a 5¼-in. floppy disk drive developed by Drivetec Inc., San Jose, Calif.

In addition, Kodak's Spin Physics Division, San Diego, founded in 1972 to develop high-density recording heads, is producing a floppy disk with a 3.3-megabyte unformatted capacity. Kodak executives say that these two products are just the start, as the firm aims its world-class manufacturing expertise at the electronics market.

"Electonics is not new to us. We just haven't stressed it," says Robert B. Seebach, manager for the 3.3-megabyte drive program. "We've tied in with existing [Kodak] technology, and have taken the tough technology in house. We've tooled some parts ourselves, and the custom chips are made here," says Seebach.

Other technologies that Kodak addresses include complex circuit-board assembly and high-volume automated assembly of consumer products such as its disk camera. It also makes ac and dc motors for slide-projector carousels, and ties control systems together with wire harness technology, Seebach notes.

Using these and its other technologies, Kodak will pursue other electronics markets, but officials won't divulge plans. Says Seebach: "This isn't a short-term commitment to electronics. We feel we have a lot to offer via pieces of the company."

Developing. "Electronics is not new for us. We just haven't stressed it," says Kodak executive Robert B. Seebach, who is in charge of its disk drive operation.

The first products from this turn toward electronics, the disk drive and floppy disk, will position Kodak in a high-density market that is expected to grow to "hundreds of thousands" of drives annually, according to industry analyst Jim Porter of Disk/Trend Inc., Mountain View, Calif. "Kodak is trying to carve out a position so it will be a leader" in this market, remarks Porter.

The system, with 192 tracks/in., is billed as having the largest capacity of any commercially available 5¼-in. floppy drive system. The drive is most suitable for applications such as medical, engineering, and business. Porter calls it a software-driven market.

Porter believes that Kodak's only other direct competitor is Amlyn Corp., San Jose, Calif., which offers a 170-tracks/in. floppy drive and a 3.2-megabyte floppy disk. "The Drivetec/Eastman Kodak approach appears to be the leader. It's a very solid offering," says Porter.

As for possible competitors in the part of the floppy disk market targeted by Kodak, according to Porter any of 20 large manufacturing companies in Japan, Europe, and the U.S. could enter the high-density market, but have chosen not to do so at this time.

Marketing of the drives is being handled by Data Technology Corp., Santa Clara, Calif., a manufacturer of disk drive controllers. A Kodak subsidiary, Atex Inc., Bedford, Mass. owns 25% of the firm.

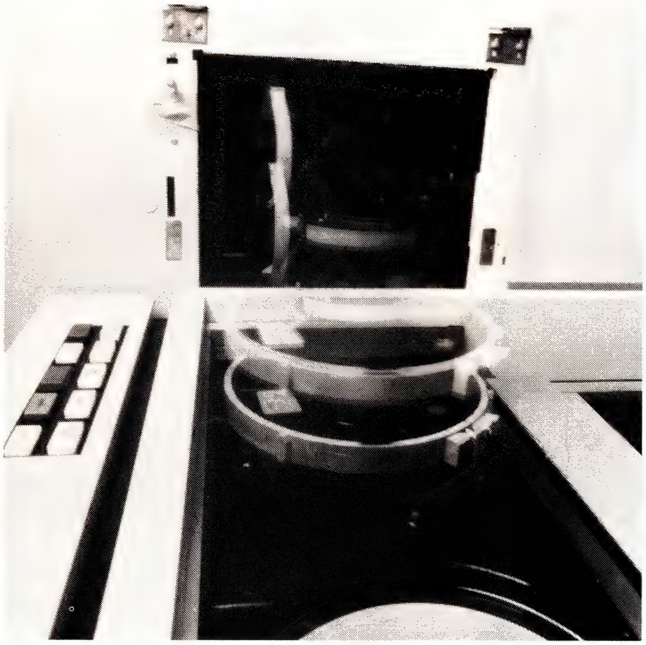
Data Technology is shipping drives at a rate of 1,000 a month, but "we expect it to do quite a bit better in the next couple of months," says Michael Kirby, vice president of marketing. –**Steve Haggerty**

Braegen International carves out own niche in European market

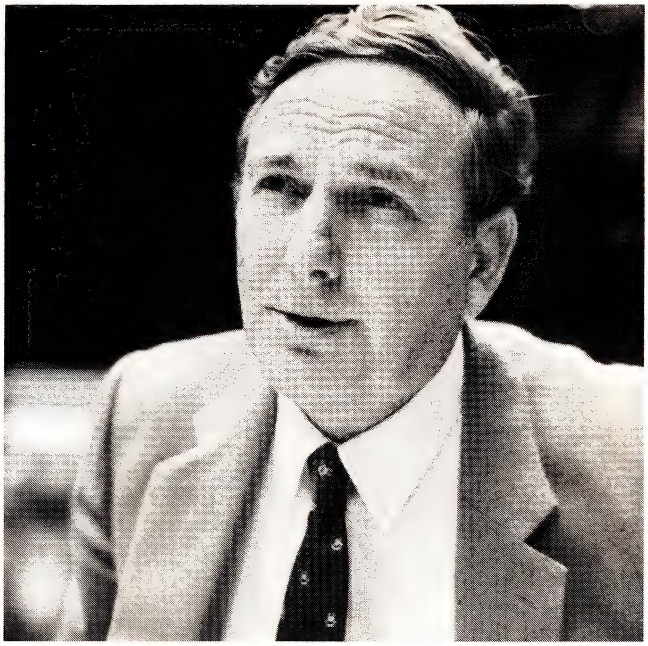
Brussels

Coming across a newly formed European firm named Braegen International, whose product line consists solely of automated tape libraries and local networks made by Braegen Corp., of Anaheim, Calif., an observer might well assume that the former is a subsidiary of the latter. However, that would be an erroneous conclusion.

"We are established as a separate, independent company," notes Alfred Heilbron, managing director of Brae-



Tape changer. Since starting business, Braegen International has had success selling an automated tape library system that utilizes standard ½-in. magnetic computer storage tapes.



History lesson. Many firms set up foreign units too quickly, notes Braegen International's Alfred Heilbron. If the parent gets in economic trouble, "the first thing they do is to dissolve the subsidiary."

gen International. "It is true that we are marketing exclusively products produced by Braegen Corp. in the U.S., but at the moment we're only one year old. On the other hand, we have the right to go outside of Braegen to find new products for our portfolio, and we have the right to start fabrication of our own products if we decide that it would be beneficial to do so."

Both firms do, in fact, have a principal shareholder in common (although the shareholder remains anonymous), as well as their name, but Heilbron notes that his firm is autonomous for all practical and legal purposes. The thinking behind establishing the firm in such a way is simple enough. With sales of some $50 million, Braegen Corp. hasn't attained the necessary size to justify a full-scale European unit.

"A lot of companies jump the gun in establishing subsidiaries, and then when the parent goes through a couple of difficult quarters with flat or dropping sales, the first thing they do to cut costs is to dissolve the subsidiary," says Heilbron. "Our independent status is a good, intelligent way of operating, because it assures our European customers that we're here to stay."

Heilbron readily admits that there are other automated tape libraries currently on the market, notably one that was developed by IBM Corp. However, all these systems, unlike the Braegen system, use tape reels of their own design. Braegen's works with standard half-inch magnetic computer storage tapes, thus giving the company an advantage in competing for those customers who already have an extensive tape library in service.

Good advantage. The firm was able to capitalize on this advantage to win its first European contract to automate the central data-processing department at the Bank of Italy in Rome.

The other key product Braegen will be counting on is a system that permits the connection of IBM System/370 mainframes and personal computers into an local network, using standard coaxial cable and connectors. Designated Elan and based on a proprietary collision-avoidance protocol, the system, stresses Heilbron, has no competitors other than full-blown LANs based on protocols such as token passing and collision detection. Those, he maintains, require an investment several times that necessary to install Elan. The company will be launching the product in Europe sometime later this month.

With a staff of only 10 involved in sales and support of the two products, Heilbron knows Braegen must choose its target markets carefully. The firm's initial effort will center on Benelux, in France, Switzerland, and Italy, with a strong possibility of dealer agreements to cover other important countries, such as the UK and Germany.

Besides its right to manufacture its own products, Braegen International is empowered to negotiate licensing agreements with other companies to manufacture Braegen products. Heilbron thinks that European distributors would be likely candidates for this role. And with the dollar currently hovering near record levels, a European source of supply must be a tempting prospect for the fledgling company. **–Robert Gallagher**

BOTTOM LINE

Financing concluded. Charles River Data Systems Inc., Framingham, Mass., has completed a third round financing that totaled $5 million. Among the investors was Datapoint Corp., the San Antonio, Texas, maker of distributed data-processing equipment and local networks. Besides investing in the firm, Datapoint will become Charles River's largest original-equipment manufacturer customer. The Texas firm will buy Charles River's 32-bit general-purpose microcomputer.

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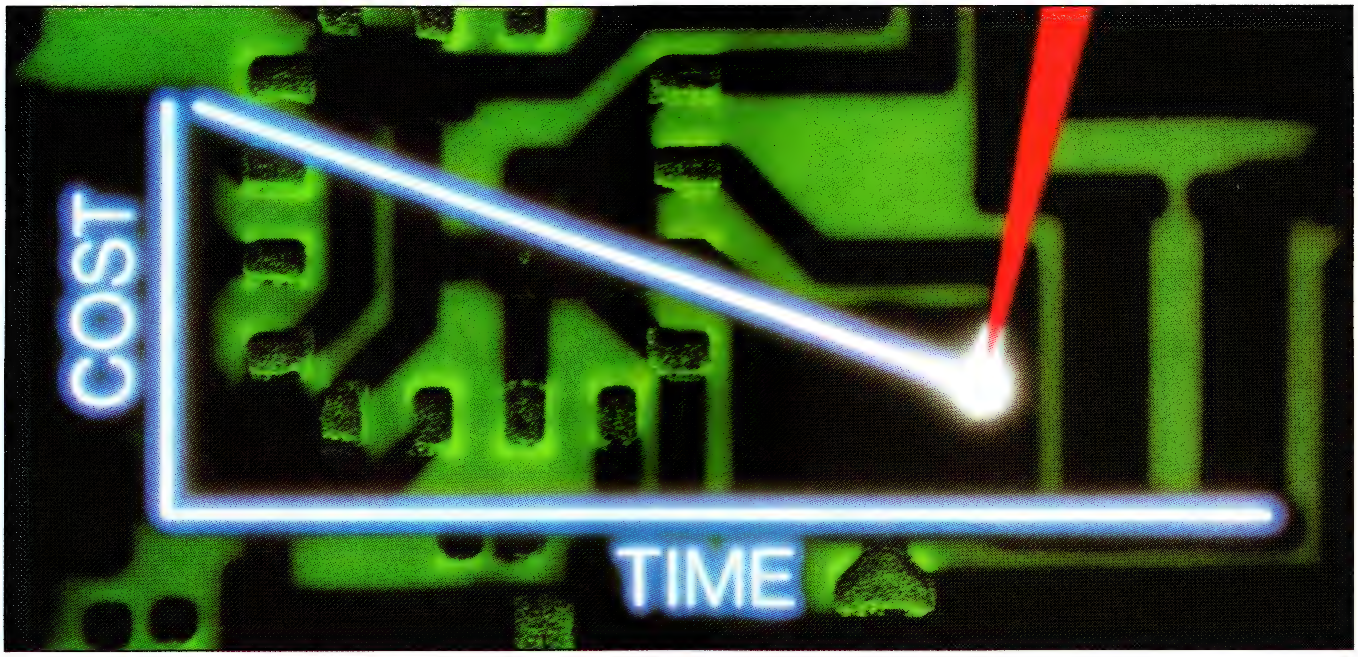

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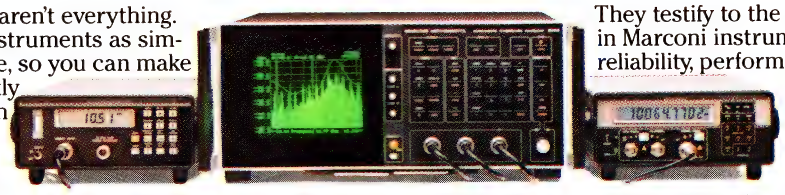
Microwave counter HP-5342A Option 011 Frequency coverage 10 Hz to 18 GHz Maximum resolution 1 Hz Sensitivity at 1 GHz −25 dBm, at 18 GHz −20 dBm Maximum input damage level +25 dBm peak Automatic acquisition time 530 ms (normal FM)	**Microwave counter** MI-2440 Frequency coverage 10 Hz to 20 GHz Maximum resolution 0.1 Hz Sensitivity at 1 GHz −25 dBm, at 18 GHz −20 dBm Maximum input damage level +27 dBm Automatic acquisition time 200 ms typical
Power meter HP-436A Option 022 Technology: TTL logic Instrumentation accuracy ± 0.5% or ± 0.02 dB ± .001 dB/C° Power range with available detectors −70 to +35 dBm Frequency range 100 kHz to 26.5 GHz Calibration: adjustment manual screwdriver Response time fixed by range Panel height 5¼″	**Power meter** MI-6960 Option 001 Technology: microprocessor controlled Instrumentation accuracy ± 0.5% or ± 0.02 dB Power range with available detectors −70 to +20 dBm Frequency range 10 MHz to 20 GHz Calibration: adjustment automatic, key or GPIB Response time is user selectable Panel height 3½″
Scalar analyzer HP-8756A Frequency range 0.01 to 40 GHz Electronic graticule; 401 point display, line only Dynamic range +10 to −50 dBm Fast screen dump and direct digital plotter output Sweeper control exclusive HPIB port to HP8350B or HP8340A Minimum sweep time 150 ms Logarithmic conversion by analog circuitry	**Scalar analyzer** MI-6500 Option 001 Frequency range 0.01 to 40 GHz Electronic graticule; 422 point display, line and histogram fill-in Dynamic range +16 to −55 dBm Fast screen dump and direct digital plotter output Sweeper control coax cable to all popular sweepers Minimum sweep time 70 ms Logarithmic conversion by digital circuitry
Price	
HP-5242A-011 Microwave Counter ______ **$ 6,850**	**$5,290** ______ MI-2440 Microwave Counter
HP-436A-022 Power Meter ______ **$ 3,400**	**$2,690** ______ MI-6960-001 RF Power Meter
HP-8756A Scalar Analyzer ______ **$11,000**	**$8,195** ______ MI-6500-001 Scalar Analyzer



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SPECIAL REPORTS

SEMICONDUCTORS PACE GROWTH OF COMPONENTS

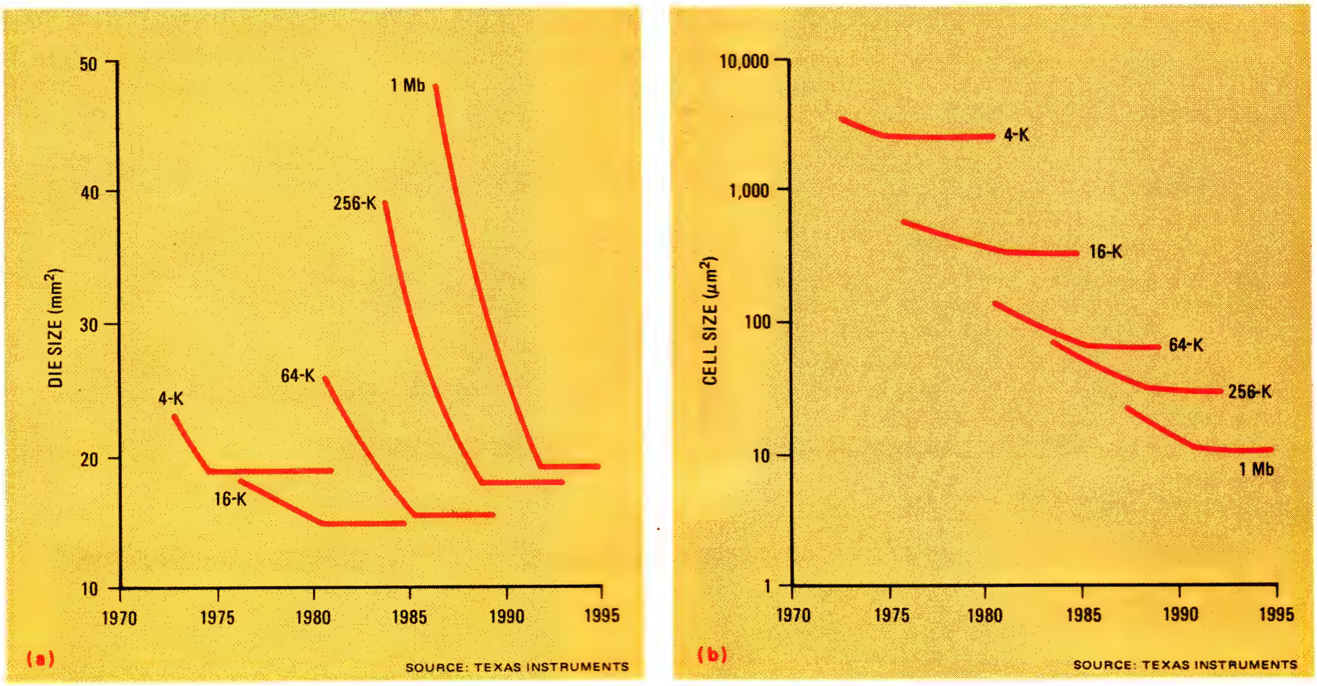
Increasing demands for choices of speed, power, and packages are turning vendors to systems approach

☐ *by Henry A. Davis*

Driven by the continuing demand for ever increasing functionality per integrated circuit, semiconductor manufacturers are turning to systems experts in order to choose the right set of features. With memory designs hitting device densities of more than a million, and microprocessors, peripherals, and interface circuits nearing half a million transistors per circuit, designers are turning to sophisticated computer-aided design systems and more regular design techniques to deal with the basic issue of chip density.

Along with increasing circuit densities comes a host of tough technical problems: increased power dissipation, longer test times, more demanding tests, packaging, higher design cost, and tighter process control. As formidable as these problems are, probably the biggest hurdle is the choice of what exactly to do with half a million transistors. To address this issue, semiconductor component designers are relying on systems experts, both in house and at customer sites. Their product specifications have already given rise to multiple data configurations for dynamic random-access memories and promise to push the semiconductor industry toward greater market fragmentation in all product areas. Specialization in the memory market is an indicator of what is to come for other categories of semiconductor products.

Historically, the memory market has been made and dominated, to an unprecedented degree, by the DRAM. Now this market is fragmenting into largely separate markets divided according to memory types: DRAMs, erasable programmable read-only memories, nonvolatile RAMs, and electrically erasable PROMS. Within these groupings variety abounds, giving the system designer



SOURCE: TEXAS INSTRUMENTS

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DRAM history. Successive generations of dynamic RAMs have improved through their life cycles to mass production in the 15-to-20-mm² chip size (a). Extreme reductions in cell size of new dynamic parts require at least halving the significant process features (b).

choices of speed, power, size, and configuration to meet specific needs.

Software has become the name of the game for virtually every systems integrator and original-equipment manufacturer. Compatibility across a variety of different systems products has become a must. This means an increased amount of pressure on the semiconductor manufacturers to produce microprocessor families that are not only upward-compatible but also downward-compatible across central processing units. With downward compatibility, designers can implement lower-cost systems by utilizing smaller data bus versions of the CPUs, while keeping true software portability.

Early microprocessor designs, whose memory-addressing capabilities were limited to 16 bits, have given way to a new breed of processor, designed in the spirit of true mainframe computers, with full addressability. Existing 32-bit machines with 24-bit addressing will be enhanced to include full 32-bit addressing much like their mainframe counterparts. Greater numbers of transistors per IC allow support of virtual memory in hardware, thus supplanting the older, and more difficult to program, memory segmentation schemes.

Microprocessors reaching limit

Unlike memories, microprocessors have an end in sight for word size, with 32 bits universally accepted by manufacturers as the maximum for a standard product. With most major manufacturers already committed to a processor family and the high cost of developing and supporting a new instruction set, the near-term end of processor offerings has been reached.

Most new work will concentrate first on integrating more support chips onto the processor and then on the area of specialized coprocessors, such as the standard floating-point processors. Peripheral products will continue to receive significant attention from both semiconductor manufacturers and system designers. Major advances in video processing technology and peripheral controllers are in the works at several firms, as support for the powerful new 32-bit processors.

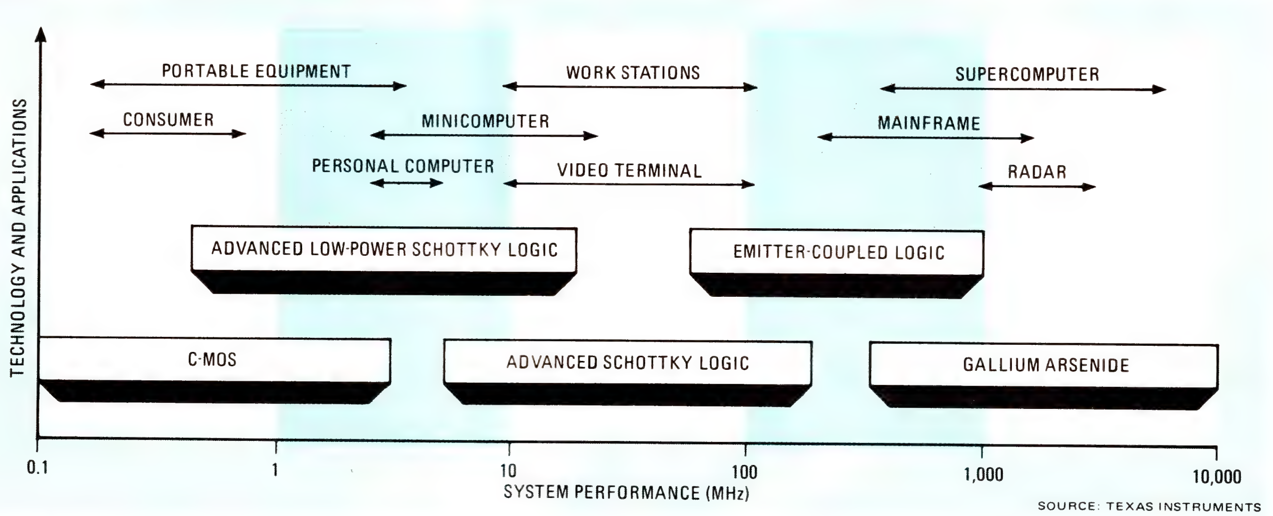
In the analog and traditional TTL markets, hot new complementary-MOS processes promise to give older bipolar processes a run for the money. Full TTL sink-and-source compatibility is now available from CMOS-equivalent parts, implemented with a new variant of the old metal-gate CMOS process. As pin-for-pin replacements for bipolar parts, these parts offer the same propagation delays as their rivals but at a lower power dissipation, giving designers an alternative that allows full operational speed for high-performance processors, but without the power penalties. (While CMOS is making its way into the analog world, bipolar is still the king of precision for operational amplifiers and other parts requiring close-tolerance resistors and high gains.)

National Semiconductor Corp., Santa Clara, Calif., has built precision 12-bit analog-to-digital converters in a CMOS process that is compatible with logic implementation using laser-trimmed resistors. Intelligent ADCs and related parts are likely to replace the expensive trimming operation in the next year. These intelligent parts will use programmable bits to select corrective components for a high degree of linearity.

Driven by the availability of improved computer-aided-design tools, semicustom and custom design approaches are finally becoming accessible to the mass market of mid-volume systems manufacturers. With the process technology lag shortened from several years to as little as six months, both the semiconductor houses and their customers can afford to utilize the relatively fast design turnaround of CAD to rapidly bring products to market.

Standard cells, a concept for over 10 years, are now a reality at most every custom supplier. Libraries of more than 300 fully characterized cells are becoming common and will continue to be refined, especially as block routers are delivered this year.

An important trend in the standard-cell library area is the inclusion of microprocessor cores. Typically an industry standard part, these cells are supported by glue logic cells as well as application-specific cells such as speech synthesis, analog circuitry, and high-density standard memories. Furthermore, EEPROM and PROM technologies are likely to be added over the next few years to the cell libraries.



SOURCE: TEXAS INSTRUMENTS

Systems trends. Technology is rapidly improving system capabilities. In order to keep up with the trend, semiconductor designers are turning to systems approaches to exploit the appropriate technologies for the specific application.

Process advances in CMOS and bipolar enhance speed and density

Usually, semiconductor technology is driven by memories and memory needs. Logic parts generally do not place as high a demand on processing and can be implemented with the geometries suitable for memories and their associated basic process (see "Playing the process game," p. 63).Yet process advances continue to improve the capabilities of logic parts. One trend is the replacement of standard bipolar parts with equivalent CMOS parts.

For example, Zytrex Corp., in Sunnyvale, Calif., using just eight mask steps in a double-metal, scaled-metal-gate CMOS process, has produced pin-for-pin, fully TTL-compatible parts that have identical or better drive characteristics than their large-scale counterparts. Gate properties such as those of silicon gate processes are achieved in the 2-μm self-aligned process. Power and ground for the devices get bussed on one level of metal, while the other level carries signals at right angles.

The process yields a 1.5-ns gate delay for a two-input gate, with a fanout of 2. Both the n and p transistors are the same size with an effective channel length of just 1.2 μm. Guard lines are used extensively in the designs to minimize latchup. On the drawing board at Zytrex are a number of large-scale-integration parts, including a microprocessor targeted at 110 mils on a side. This compares with 180 mils for its bipolar equivalent.

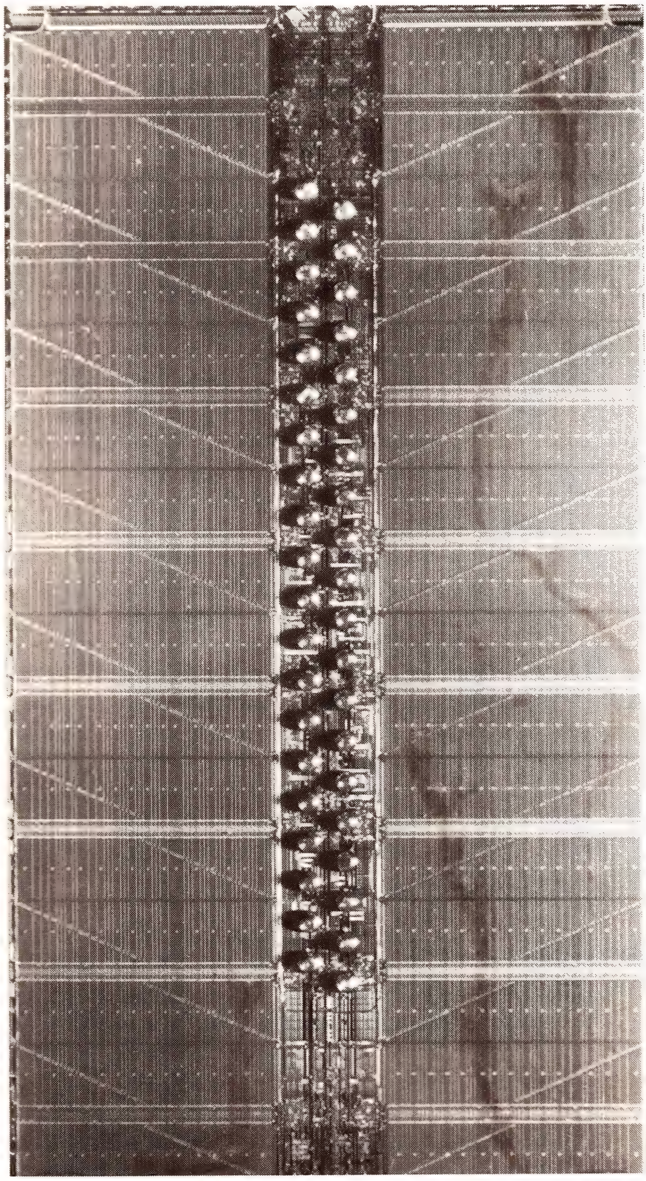
Bipolar upgrades

Meanwhile, bipolar processes are going through upgrades to make switching times even faster. Standard TTL components, though upgraded as the process is improved, are based to a large extent on process technology that is more than 10 years old. Still, the faster switching times and lower power consumption of advanced low-power Schottky, advanced Schottky logic, and Fairchild Advanced Schottky TTL are squeezing the older bipolar families out of new designs as well as out of many existing sockets.

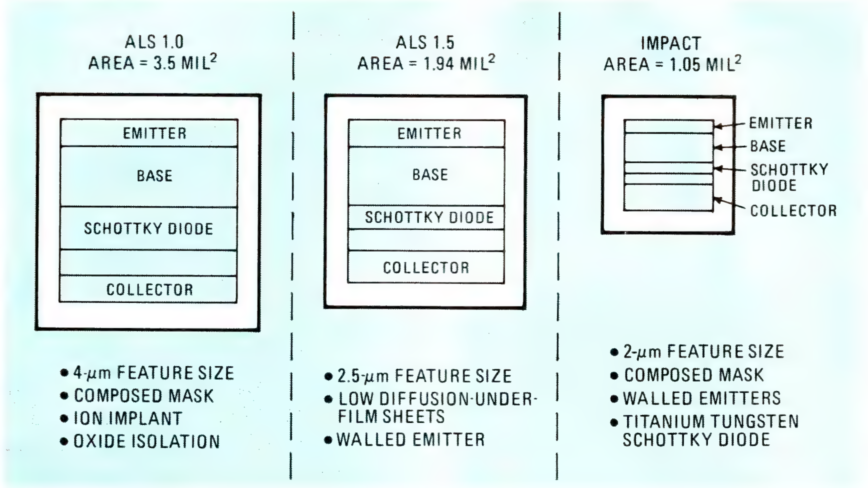
Clever circuit design in Texas Instruments Inc.'s Impact lines allow internal feedback to compensate for driving backplanes and similar loads with minimal edge rates while still meeting speed requirements. The Dallas firm's approach uses internal compensating diodes to kill supply current spikes and pnp inputs to reduce input current loading. The standard bipolar process for ALS and AS work with 4-μm feature sizes and densities of about 3.5 mils^2 per transistor. The new Impact technology pushes the feature size down to 2 μm with 4 μm metal pitch. This improvement in the process yields transistors that fit into a chip area of just 1.05 mils^2.

Read-only memory products continue to lead the technology in memory size, with 1-Mb chips now out. Ultraviolet erasable programmable ROMs are on their way to 512-K, with 1 Mb just around the corner. Both MOS EEPROMs and their bipolar cousins have reached the 64-K level, to the surprise of early market watchers. Nonvolatile RAMs have reached the 4-K level and are establishing themselves as a workable product.

Despite their position as the density king of memories, ROMs continue to have significant drawbacks for the



Forerunner. This 256-K dynamic RAM chip now in production by IBM probably is a model for a forthcoming megabit RAM in development. This chip measures 5.13 mm by 9.85 mm. The odd structures in the center are solder bumps for mounting on a ceramic substrate.



Bipolar lives. TI's bipolar process migration for logic has reduced transistor area by more than a factor of three and feature size to 2 μm. The advanced bipolar processes, like their MOS counterparts, require direct step on wafer to achieve process repeatability and yield.

systems designer, namely the chip's inherent unalterability. With 1 Mb of program space, software errors have become a major concern for any company; in 128-K bytes, programmers can expect from 30 to 300 errors.

Toshiba Corp., Kawasaki, Japan, turned to a p-well CMOS static circuit to produce an 80-ns, 1-Mb ROM. Individual memory cells are packed into an area less than 34 mils² using 2-μm design rules. The high speed comes from a combination of sense-amplifier design and reduced parasitic capacitance at the sense nodes.

To handle bit errors in ROMs, Oki Electric Industry Co., Tokyo, turned to a fully redundant ROM design for their 1-Mb chip. Four times as large as a standard nonredundant ROM, it has an access time of 10 μs. Laid out in n-MOS, the circuit uses relaxed design rules intended to not push the process technology. Using this experience and advanced lithography techniques, Oki claims to have developed and completed pilot production of a 4-Mb ROM in a joint effort with Nippon Telegraph & Telephone Public Corp.

Motorola Inc., Schaumberg, Ill., handles ROM customization by mixing ROM and EEPROM technologies. The combination part comes in two different versions, depending on whether programmable redundancy is desired. Both parts are compatible with 128-K ROMS and EPROMS and have a static power-down mode that is enabled by selecting both output-enable and chip-enable high. While the MCM836E16 is configured as 16-K-by-8-bit chip with 2-K of EEPROM and 14-K of ROM, the MCM6836R16 adds a 256-byte memory block that can replace a 256-byte block in either EEPROM or ROM.

Improved wafer yields

Error-correction circuitry expanded Hitachi Ltd.'s 1-Mb ROM by about 20% and lengthened access times, but allowed improvements in wafer yields of almost 300%. Arranged as a 32-bit-wide array, the ROM needs six check bits to fully correct single bit errors in about 15% more time than the uncorrected ROMs.

Mostek Corp., Carrollton, Texas, plans a 1-Mb ROM in a 64-K-by-16-bit configuration for the new generation of processors. The proposed 28-pin package would accommodate even larger chips when they arrive. Emitter-coupled-logic technology with access times of 10 ns keeps bipolar processes at the forefront for fast PROM products. The less exotic TTL technology has about half the speed of ECL, with smaller PROMs in the 20-ns range. Large arrays up to 8-K by 8 bits have typical access times of 40 to 70 ns while consuming under 1 W; low power dissipation is generally achieved in the standby cycle. The tough design problem is minimizing delay paths through the chip's periphery.

Vertical fuse structures used by Fairchild Camera & Instrument Corp., Fujitsu, and Signetics rely on a diffused eutectic aluminum process and oxide-isolated transistors to short-circuit the transistor junction during the programming process. A high current is passed through a forward-biased junction of the programming transistor to achieve the aluminum migration. This technology will lead to 64-K PROMs, which will reach the market in 1985.

Raytheon Co., Lexington, Mass., uses amorphous silicon to program its vertical fuse structures with less than half the current of other approaches. Production on a 16-K PROM is expected to begin by the end of the year. Combined with oxide-isolated transistors, the amorphous silicon approach could make it possible for designers to fit a 64-K PROM into just 40,000 mils².

An experimental 1-Mb EPROM from NEC Corp., Tokyo, uses advanced lithographic techniques to achieve 1.2-μm design rules on a par with very high-speed integrated-circuit processes. The chip can be used in either an 8- or a 16-bit bus system by using a bus control pin. Though the 1-Mb level in an EPROM is impressive, only Intel Corp., Santa Clara, Calif., and American Micro Devices Inc., Sunnyvale, Calif., can deliver products at the 512-K level. Both companies use plasma etch in a 2-μm process.

Seeq Technology Inc., San Jose, Calif., uses a 1.5-μm CMOS to build its 256-K EPROM. With programming voltages in the 12-V range, the part can be programmed in about 500 μs per byte. An epitaxial layer minimizes noise and latch-up risk in the two-polysilicon-layer, n-well process. Toshiba will release a comparable part this year using 2-μm design rules. Access time is 100 ns compared with Seeq's 125 ns, but the chip is 75% larger. A self-aligned diffusion in a p-epitaxial layer is used for both the memory element and the sense amplifier. Intel and NEC are working to produce on-chip charge pumps as a way to eliminate the multiple voltages required for programming. Since the floating gate construction requires little current for programming, success in the next few years is likely.

Meanwhile, Oki is attempting to make plastic parts with an erasure window, as a cost reduction strategy. Thermal mismatch has always been a problem for plastic EPROMS, but with good hermetic plastics available, the goal appears attainable.

Playing the process game

While this article makes constant reference to feature sizes in various processes, there has always been a debate concerning what constitutes the size of a process. Many, but not all, manufacturers refer to gate dimensions as the primary feature. In this sense, it is possible to have a gate with a 3-µm drawn line produce a 2-µm etched line and a 1-µm line after further processing. These different measures are generally referred to as drawn, actual, and effective. How a particular manufacturer describes his process depends on the intended use and how it is to be marketed. Few suppliers use drawn size as their stated measure, since printing and etching steps can make a substantial difference to the circuit. Conservative measurements deal primarily with actual gate width while more aggressive marketing will refer to effective gate width. Occasionally, both figures will be given so that it is easier to compare processes.

The measure of interest depends largely on the intended use of the process. Small effective lengths will yield a faster transistor but will not affect die size, while finer line widths will achieve a smaller and faster part. Gate size in most chips contributes relatively little to circuit area and is therefore, from a size standpoint, not important. Examination of actual circuit layouts shows that for newer designs, upwards of 85% of the device area is frequently consumed by interconnection metal. Thus, while gate width is important for speed issues, the size of interconnecting lines determines die size. Simply measuring metal line width is not sufficient, since there must be a space between metal lines.

Pitch refers to the distance from one edge on a metal line to the corresponding edge on an adjacent line. This size directly affects the number of gates that can be placed on the device. A process that has 3-µm metal lines but 4-µm spacing has a 7-µm metal pitch.

To see how pitch affects die size, consider two competing processes: one with 3-µm gates and 7-µm pitch, the other with 2-µm gates and 6-µm pitch. Both processes could have the same effective gate size and therefore the same speed, but the real difference is in chip area. While gate area reduces in size from 9 to 4 mils^2 (55%), the chip area will only see a 27% (49 to 36 mils^2) reduction.

Circuit shrinks are sometimes offered as an upgrade path for new processes. However, there are penalties associated with designing a shrinkable process. In order to shrink, which is a purely optical procedure, the original circuit must be made oversize in several areas. First, pads must be sized up according to the shrink factor; a 50% shrink to yield a 4-mil pad requires the drawn pad to be 6 mils. Second, a 3-µm and 2-µm process pair usually does not shrink all dimensions equally well. Staircase effects of successive etching steps on the surface of the die precludes linear reductions in line spacing and widths for optimal processes. The result is that the original circuit must be made oversize relative to the 3-µm process in order to shrink to the 2-µm process optimally.

Smaller line widths do in fact have benefits even when they are not coupled with reduction in spacings. Smaller line widths means more open space on the die and therefore a better yield as compared to the same pitch with larger lines. Sometimes, as in the case of gate arrays, the goal of finer lines is to reduce gate lengths even though the overall die size remains unchanged.

Other approaches to minimizing die size include multiple layers of metal and silicides for poly interconnect. While silicides reduce the resistance of poly by a factor of 10, metal is still lower by another factor of 10. For this reason, and process simplicity, many manufacturers are providing double- and even triple-level metal. The drawback to multiple layers of metal is the increasing pitch for each metal level due to staircase effects.

For CMOS, increasing emphasis is being placed on stacked transistor arrangements. This eliminates both a transistor and interconnects from the planar area. Bipolar has used silicides and multiple levels of metal for more than a decade. Like MOS structures, metal pitch has an important effect on die size. Performance, however, depends mostly on base-emitter spacing, base resistance, and junction capacitance. Most approaches to lowering capacitance use sidewall oxide isolation and poly. Resistance can be lowered by moving the base and emitter closer together.

EEPROMs were an apparent oddity in the memory race for many years. While an important technology, EEPROMs had significant problems of slow access times and the need for multiple power supplies due to the p-channel metal-nitride with which they were implemented. N-channel and silicon gate technologies allow EEPROMs to achieve reasonable access times and to use fewer power supplies. Still, EEPROMs use at least twice as much silicon area to implement each memory cell, when compared to EPROMs.

Exel supplies a fast (55 ns) 32-K CMOS EEPROM that competes favorably with bipolar access times. Active current (90 mA) is about half that of the bipolar part. Though only 100 storage cycles are possible, it is still an effective PROM replacement.

On the other end of the spectrum, Seeq has incorporated an error-correction circuit into its design to permit up to 1 million write cycles. Theoretically, the circuit could be programmed as many as 10 million times. Incorporating such circuitry levies a 20% area penalty, though access time reaches a respectable 100 ns. The process relies on an 85-Å tunnel and 400-Å interpoly dielectric to give short programming times of 1 ms per byte.

In the 10,000-storage-cycle range, several manufacturers are competing with products having varying system features. NCR Corp., Dayton, Ohio, uses a 16-byte page register to allow up to 16 bytes to be written in 10 ms. Motorola has no page register but offers an access time of 150 ns, almost twice as fast as the NCR part.

Hitachi addresses the issue of programming time by implementing their 64-K EEPROM with very thin oxide and double implants in the source and drain for higher breakdown voltages. The higher breakdown voltage drops programming time to just 2 ms, including erase and write. Inmos Ltd., Bristol, UK, chose to add a dedicated processor to their 64-K part to control operat-

He started MOS from scratch

Some 21 years ago, Frank Wanlass literally scratched out the first reliable MOS transistor with a tungsten wire. Today, he is still hard at work establishing MOS as the most versatile technology for making semiconductors.

In 1963, MOS was a curiosity. The first circuits, made by RCA Corp., New York, from cadmium sulfide and cadmium selenide, were notoriously unstable. Wanlass, a freshly minted PhD out of the University of Utah, Salt Lake City, was at the legendary Fairchild Camera and Instrument Corp. research lab in Mountain View, Calif., trying to duplicate the RCA circuits in silicon, with small success. Fairchild had the newest electron-beam evaporation equipment, and someone had coated a wafer with platinum, which cannot be etched. In desperation, Wanlass used a fine tungsten wire to draw the circuit by hand—and it worked.

Encouraged, he fabricated some circuits from aluminum, which had previously been suspected as a source of contamination, and found that they worked too. "It turned out that the contamination had come from the sodium, which had been used to coat the filaments that were previously used in evaporation," Wanlass recalls. "Sodium was the culprit that was causing the gate region to drift. That was the first breakthrough in MOS."

It was immediately obvious, Wanlass says, that if p-channel devices could be made, n-channel devices were also possible. He began developing the idea of complementary-MOS logic, and received the first CMOS logic patent. He was supported at first by Gordon Moore, his boss at Fairchild research and development, but the management at Fairchild—then at the top of the heap with its bipolar DTL logic—wasn't interested. After a while, Moore wasn't either, and eventually Wanlass went looking for a company that was. It is ironic, he feels, that five years later, Moore went on to help found, along with Robert M. Noyce, another Fairchild alumnus, the Intel Corp., which built its success on MOS, while Fairchild has floundered in this market.

Wanlass's odyssey began somewhat inauspiciously at General Microelectronics (later Philco-Ford Microelectronics), which ran aground on the shoals of the Victor calculator. This revolutionary design was based on the first commercial MOS large-scale integrated circuit, a 20-bit shift register. Philco-Ford couldn't make the circuits reliably, and eventually fled the IC business altogether. Wanlass moved on to the General Instrument Corp., New York, where he developed a thick-oxide process that eventually became an industry standard, and a nitride process that allowed MOS to interface directly with TTL.

Subsequently, Wanlass founded four other MOS firms, developing *en route* processes for CMOS watch circuits and electrically alterable circuits. He always looked for more speed, chasing applications that were believed to be the sole property of bipolar ICs.

At his newest firm, the three-year-old Zytrex Corp., Sunnyvale, Calif., he thinks he has caught up at last. Zytrex specifies its high-speed CMOS devices, built with an eight-mask process developed by Wanlass, as pin-for-pin replacements for advanced TTL parts, and has even advertised itself with the slogans, "Who shot Schottky?" and "Bipolar bites the dust." MOS technology, Wanlass believes, can now replace bipolar in most applications. But after 21 years, he's still willing to wait a while. "There's a lot of inertia in the bipolar camp," he says. "It won't go away overnight."

–Clifford Barney

ing modes and support a 64-byte page register for 64-byte writes in 10 ms. Exel gives the user a control register with which to configure the programmability of the 64-K chip.

NVRAMs are too new in the market to accurately predict their future. Large NVRAM arrays are mostly in the 4-K range. Mostek bucks the trend of solid-state solutions with their hybrid technology. Using a CMOS RAM and lithium batteries housed in a single DIP package, the 16-K part is by far the densest available and has a 10-year data retention life. Next year, the manufacturer will introduce a 64-K NVRAM well ahead of competing approaches to nonvolatility.

Static CMOS RAMs continue to push speeds down into the bipolar range, while bipolar speeds continue to improve. A host of start-ups are pushing processing to the limits, to make 35-ns and faster parts available in CMOS. Cypress Semiconductor, San Jose, Calif., has the unquestioned lead in the fast CMOS memory arena with 15-ns parts. Available in 256-K-by-4-bit, 16-K-by-4-bit, and 1-K-by-4-bit configurations, the parts all use 1.2-μm geometries to achieve their speed. Similar-performance chips of 4-K by 1 bit and 2-K by 8 bits will be available soon. Meanwhile, in the larger memory sizes, Integrated Device Technology, Santa Clara, offers a variety of 64-K parts ranging in speed from 55 to 85 ns and 16-K RAMs at 45 ns; with the new processing to come on-line next year, 64-K parts will shoot into the 35-ns range.

Gallium arsenide may well be the technology of choice for SRAMs where the ultimate speed is required. GigaBit Logic has developed a 1-ns, 1-K RAM using depletion-mode field-effect transistors fabricated by direct implantation into semi-insulating GaAs. The use of semi-insulating materials decreases parasitic capacitance and eliminates isolation junctions, increasing speed and yield.

DRAMs continue to be a primary process development vehicle in the U.S. The development frontier at the moment lies at the edge of 1-Mb RAMs. Although some firms have shown developmental prototypes, the bigger memories are at least two years away from production. IBM Corp. has shown a laboratory version of a 1-Mb RAM; the part was fabricated on the same line in Essex Junction, Vt., that produces the recently announced 256-K DRAM used by IBM in its 3880 storage control unit.

Chip dimensions of 10.5 by 7.7 mm for the 1-Mb unit were achieved thrugh the use of 1-μm versions of IBM's silicon and aluminum oxide process. Electrical isolation of adjacent storage nodes and a thin dielectric of just 15 nm increase the amount of charge stored per unit area. By the end of 1985, Intel plans to have samples of a 1-Mb part using 1-μm CMOS process featuring 100-Å oxides. One major issue in the 1-Mb race is the package's shape and size. Two proposals are on the table, one for a square leaded chip carrier and another for a skinny dual in-line package.

In the area of 256-K n-MOS DRAMs, Motorola has switched from a part designed with silicides to a triple-polysilicon process. With the 256-K part, the MCM6256, Motorola joins National Semiconductor in the triple-poly camp. Intel's 256-K part is their entry into the CMOS DRAM market. Using their advanced process called CHMOS-III-D, a 1.5-μm, n-well process utilizing 250-Å gate oxides, the Intel part features fast ripple and static column modes that result in almost a fourfold improvement in access time to 15 million bits/s [*Electronics*, June 14, 1984, p. 138].

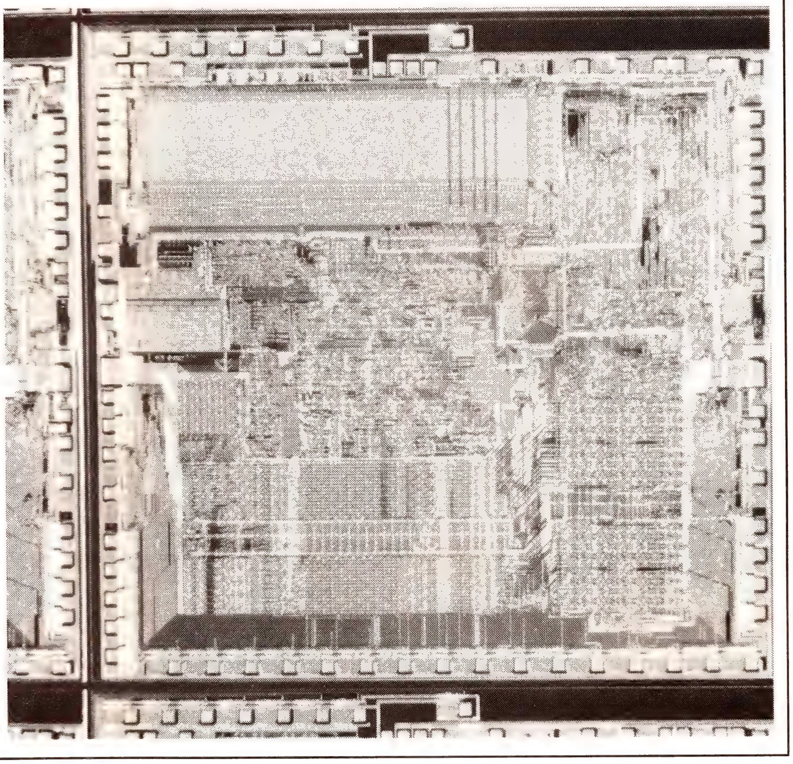
The resulting design uses one twentieth the current for data retention as compared to existing n-MOS designs. The process, which keys off Intel's HMOS-III standard, requires the use of direct-step-on-wafer and dry-etching processes. A p-type epitaxial layer on a heavily doped p-type substrate hosts an n-well to solve latchup and allow for the more compact n-channel memory arrays. Use of an n-well makes very low soft error rates possible.

MICROPROCESSORS AND PERIPHERALS

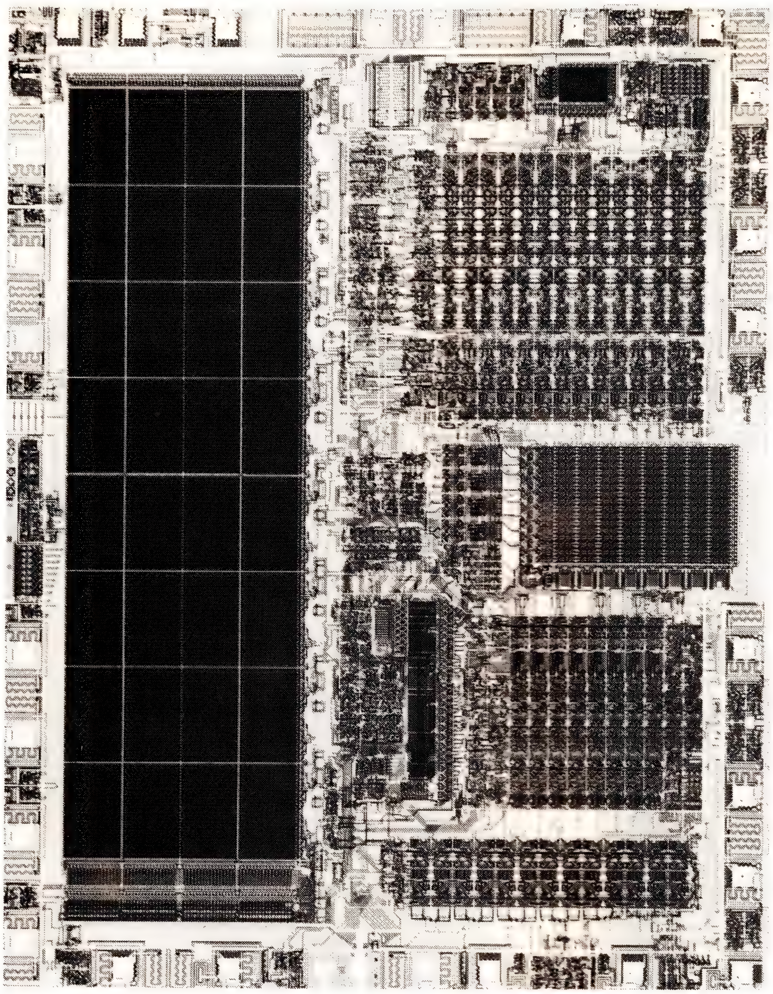
Competition—and technology exchange—heats up in the 32-bit microprocessor arena

With National Semiconductor Corp. and Texas Instruments Inc. joining forces in a technology exchange, the National 32000 family made its bid for a share of the emerging 32-bit microprocessor market. The 32000 represents a unique break with the past.

For its entry into this highly contentious arena, National followed the dream of every chip architect: a clean design based solely on technical considerations, and not beholden to previous generations. The result is a family of processors that are upward- and downward-compatible with previous processor generations, with full 32-bit features. The Santa Clara, Calif., company took somewhat of a risk in choosing to delay the introduction of parts until the complete package—support software; timing circuit; interrupt controller; and memory-mapping, floating-point, and central processing units—was available. The follow-on advanced CMOS processor, 32432, is scheduled for availability during the middle of 1985. TI's signing on as the first alternate source assures customers of reliable supplies of the processor and its support devices. The second-source deal covers all National 32000 parts, as well as the right to



Full measure. Although late entering the market, National Semiconductor Corp.'s 32032 was the first full 32-bit design to be offered. The chip relies on a single 32-bit data bus to route data to user-accessible and internal registers.



Talker. This speech chip is representative of the new wave in microprocessor peripherals. Consisting of a reduced instruction set computer (RISC) and specialized speech processor, the device offloads a specialized function from the main system CPU.

remarket or manufacture software and systems support. The Dallas firm will be adding peripherals to the line but has not yet revealed what is on the drawing board. Both companies have adopted a kit approach to the product line in which one vendor can supply all components.

Motorola Inc. redesigned the layout of the 68020 32-bit processor in midstream, using about 20% p-type transistors after determining that the part would run too hot. Still, the Austin, Texas, design group came in within four months of schedule and produced a part that will operate consistently at the design goal of 16 MHz, with parts binning out at faster speeds. Incorporating a 256-K-byte on-chip cache, the 68020 can take advantage of program locality to speed up execution of loops and also minimize the effect of wait states.

8-bit partners

In the 8-bit processor area, Gould AMI, Santa Clara, Calif., teamed up with Zilog Inc., Campbell, Calif., to produce a combination Z80 and read-only memory to help minimize system costs. The part, designated S83, contains personal CP/M in ROM code. Custom coding can also be programmed into the masked part.

Motorola Inc. took a different approach to system cost in producing the 68C11, a single-chip microcomputer. Designers at the Semiconductor Division in Phoenix recognized that the majority of silicon area was consumed by interconnections. In an effort to shrink die size, the design team made the CPU bus interconnections in serial form, with a resulting drop in die size to less than that of many 4-bit microcontrollers. About 15% of the 68C11's area is dedicated to interconnects, in comparison to more than half for other processors. The chip has 512-K bytes of electrically erasable programmable ROM, 4-K ROM, 256-K bytes of random-access memory, 8-bit analog-to-digital converter, and four input/output ports, all contained in the equivalent of 75,000 transistors. Because the part is made with Motorola's EEPROM process, the ADC can take advantage of the double poly to make capacitors in a poly-poly configuration. The poly-poly capacitor eliminates parasitic capacitance to the substrate, thus gaining better power-supply noise rejection.

Peripherals are becoming intelligent. National currently uses laser-trimmed resistors for its 1205 12-bit ADC. In the future, the trimming operation will be replaced by more on-chip intelligence. The 1205 is representative of a trend toward adding digital circuitry to what has previously been only analog. TI has a new speech-processing chip that combines an 8-bit controller, voice-synthesis controller, 64-K ROM, and 32-K bytes of RAM, all on a single CMOS chip. The part, not yet in production, features oversampling capabilities and variable frame rates for better-sounding speech.

TI also developed an application-specific processor for telecommunications. The integrated circuit consists of over 140,000 transistors in a 2.4-μm n-MOS process featuring 400-Å gate oxides. TI's strip-chip architecture technology allowed designers to fit a 16-bit CPU, 1,408-by-18-K data memory, and error-detection circuitry onto the 114,000-mil^2 chip.

Companies such as Motorola and National hold a distinct advantage over one-process houses in the high-speed peripheral area, where both MOS and bipolar technologies are required to achieve both speed and power. National has developed a four-chip set for hard-disk control. The data separator/disk-pulse detector is implemented in bipolar using oxide-isolation for the 5-V part. For low power consumption, CMOS is used in the encoder/decoder and disk data controller.

Memory management has become an increasingly important issue for the new 32-bit processors. While National brought out a traditional virtual-memory controller right out of the chute, Motorola chose to delay the introduction of its part until the middle of 1985. As a result, there has been a proliferation of memory-management devices for the 68000 family. In addition to the three that will be offered by Motorola—the 68451, 68851, and an M68KVMMB board—second sources for the CPU have announced their own memory managers with different features. Signetics is using 2.5-μm CMOS to produce a family of memory controllers. One part services the 68010 and the other the 68020, but both have over 90,000 transistors. A third chip will be sampled before the end of the year—ahead of Motorola's mid-1985 target.

In the 68000 family, Mostek Corp., Carrollton, Texas, announced the 68200, a single-chip microcontroller based on the 68000 instruction set. Because the instruction set is not 100% compatible, the part is not regarded by Motorola to be in the family. Nonetheless, the part is significant if only for its capabilities. Implemented in CMOS, the part executes a 16-bit add in just 500 ns and fits into a 48-pin dual in-line package.

Other specialized functions are forthcoming from a variety of vendors. While not pushing process technology, the parts do offer significant benefits to systems designers. Gould and Motorola both offer bandpass, low-pass, and high-pass programmable filters in CMOS, many of them subsets of telecom parts introduced some years ago. High-precision filters, impedance matching, quality operational amplifiers, and high-speed circuitry are among the demands placed on any company wishing to offer such parts as single chip codecs and modems.

ANALOG

Packages and performance considerations motivate new design approaches

Auto-zero, analog-to-digital, digital-to-analog, and related sample-and-hold parts moved forward as a group. Complementary-MOS a-d converters are taking advantage of switched-capacitor techniques to offer auto-zeroing and calibration.

EG&G Reticon of Sunnyvale, Calif., is using n-MOS in a 10-bit ADC, the R5640, which features a switched-capacitor anti-aliasing filter and uses a charge-pump negative-bias generator to handle ±5-V signals while operating from a single supply. The n-MOS process includes double poly so that high-precision capacitors, typically matched to within 0.1%, can be made.

National Semiconductor Corp., Sunnyvale, will announce a 12-bit, 100-μm ADC with on-chip sample and hold this year. Operating from a single 5-V supply, the part will be fabricated in CMOS and come in both 12-bit and 8-bit bus versions. The ADC910 from Precision Monolithics Inc., Santa Clara, Calif., also features dual bus configurations, but is made in a bipolar process to achieve a 6-μs conversion time. External precision references allow control of the reference voltage and clock. Texas Instruments Inc., Dallas, introduced an a-d, d-a pair for their TMS 320 digital signal processor. Fabricated in n-MOS, the chips include filtering with 16-bit monotonicity, resolution and differential linearity. For the DAC, TI uses a (sin x)/x correction filter and a smoothing low-pass filter. The a-d part uses the same low-pass filter for anti-aliasing.

Processing geometries in the bipolar parts are following a downward trend similar to that of MOS. TRW Inc., Cleveland, is moving from a 2-μm single-metal-layer, triple-diffused bipolar process to 1-μm double metal. Motorola Inc.'s Semiconductor Division in Phoenix, Ariz., is reworking parts from its 5-μm emitter-coupled-logic process to the newer MOSAIC process with 1-μm features. Tektronix Inc., Beaverton, Ore., is using gallium arsenide to produce 5-bit performance with efforts continuing in the pursuit of the full 8-bit range.

High-pin-count parts in digital components have forced a move to more space-efficient leaded chip carriers and pin-grid-array packages. As a result, many companies are spending more on discrete packaging and repackaging than they are on basic device development. The chip carrier diodes from Motorola, power single in-line package from Panasonic Industrial Co., Secaucus, N.J., and other chip-carrier discretes allow tighter packing, and in many cases, autoinsertion.

Packaging continues to be the limiting factor in power devices. New packages from Motorola allow increased dissipation in support of higher current devices: they became the first supplier of VDE (European safety standard) approved triacs with the introduction of their 450-V part. Siemens AG, Munich, nearly doubled the current capability of its thyristor line with the BSt U 68H.

The increased current and voltage capabilities come from a combination of a large silicon wafer and a ceramic package 150 mm in diameter. Termed a hockey puck because of its thick disk shape, the package is used by a number of manufacturers. Siemens puts a phase-controlled silicon controlled rectifier into a 36-mm disk for their model 240. The part commutates 255 A average and 4,500 surge. On the high end, the 350 handles 350 A average and 7,500 surge and is rated to 600 V. Power Semiconductors offers a 122-mm hockey puck for its J3000. A hefty 3345-A root-mean-square can be controlled by the device with higher dc levels possible through the use of water cooling.

Westinghouse Electric Corp., Pittsburgh, offers a high-rating, fast turn-off SCR in a 100-mm puck (TA2F). The part turns off in just 40 μs and can handle 1,400 A average at a maximum 1,800 V. While the package is very efficient for heat transfer, it consumes a large amount of space and is difficult to mount—Siemens' Bst U 68H, for example, requires 15,000 lb of contact pressure. Stud-mounted devices are easier to package in a system but offer lower dissipation characteristics. Westinghouse offers a T700 series that handles up to 550 A rms at blocking voltages of 2,200 V.

Power MOS FETs are gradually catching up with bipolars in market share, but the MOS FET's on resistance leads to greater power losses than for bipolars. Their advantages: ease of drive, due to their high impedance; faster response, since they are not burdened with minority-carrier stored charge like bipolar; and freedom from secondary breakdown, so maximum operation is governed only by permissible power dissipation.

Motorola is using TMOS and CMOS to produce its SMARTpower product line. One part, the 2005, employs CMOS circuitry to control temperature and voltage sensing on a TMOS power device. The TMOS transistor has a square-shaped active area, unlike the triangular-shaped HEXFET and TEXET devices offered by International Rectifier Corp., El Segundo, Calif., and it features vertical drain current flow. Capable of handling current of up to 15 A continuously, these TMOS devices are vertical MOS structures designed to replace the bipolar devices in earlier high-power control circuits.

Switching regulators in the 10-to-150-W range are forthcoming. Low on-resistance MOS FETs from Siemens use submicrometer channel lengths to achieve maximum on resistances of 0.2 Ω. RCA has produced a series of logic-level MOS FETs using a 5-V gate drive. Devices range from 1 A at 200 V to 12 A at 100 V.

A new type of power device aims to overcome the relatively high on resistance of MOS FETs and high base current requirements of bipolar transistors. General Electric, RCA, and Motorola all produce devices that use a process similar to that of MOS FETs but adds an n epitaxial layer grown on a p substrate to eliminate much of the on resistance. To achieve the reduction, excess holes and electrons modulate the epitaxial region conductivity.

APPLICATION-SPECIFIC ICs

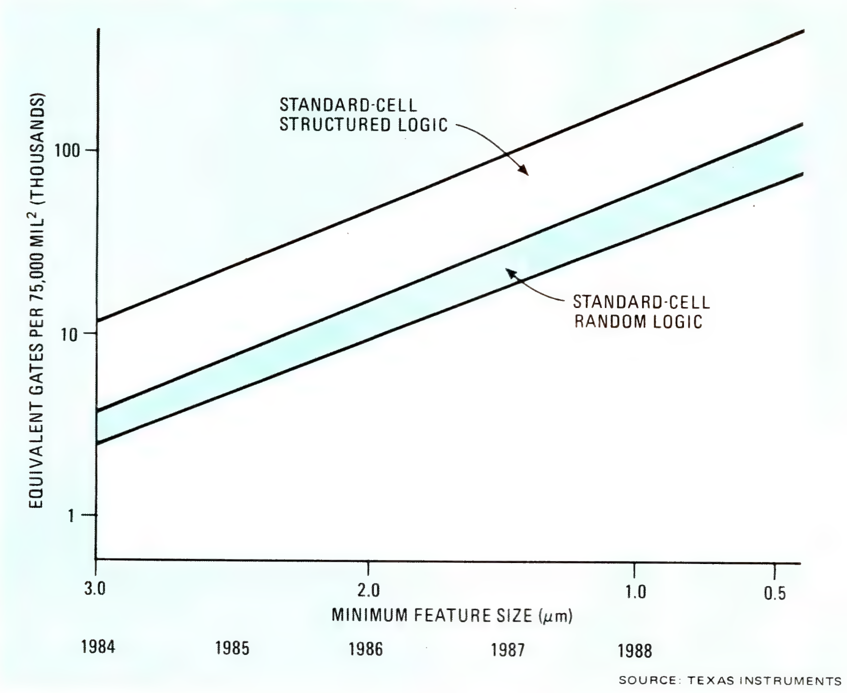
Improved computer-aided-design tools mark custom-integrated-circuit progress

Custom integrated circuits are losing their reputation for riskiness and long development times. Full hand-drawn custom layouts are still done for very high-volume consumer electronics parts, but premier value-added manufacturers can now use the same technology with much lower risk.

Computer-aided-design systems like Daisy, Valid, Mentor, and computer-aided engineering allow systems designers to become silicon designers with a minimal training. Perhaps more important for the designer, databases are portable from one manufacturer to another, giving true second sourcing at the design level. Gate arrays in complementary-MOS and bipolar provide a quick and relatively low-cost entry into custom design. Typical design tools include macro libraries of standard TTL functions that can be specified by the designer, and standard cells to allow the designer to implement more efficient devices, though they entail additional masks that add cost (Fig. 5).

However, most standard cell manufacturers have added processor cores and other big building blocks to their systems. ZyMos Corp. brought the Intel 80C49 core to its family as a result of a cross license. Motorola Inc. and Gould-AMI, among others, are adding the basic elements of their standard product offerings to their standard cell libraries. Analog components, switched-capacitor filters, LPC-10 filters, erasable and electrically erasable read-only memories, memory blocks, and other specialized functions round out many libraries. Unlike gate arrays, standard cells are not very portable between vendors, but with the flurry of cross-licensing between companies there should be no problem in finding a second source for any given design.

One of the most powerful forces in



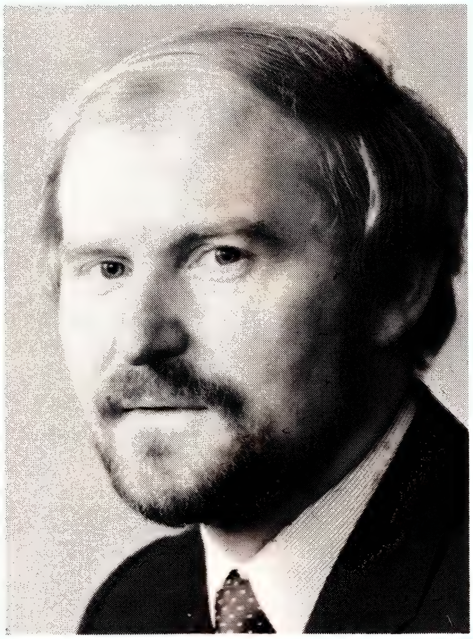
SOURCE: TEXAS INSTRUMENTS

5. Semicustom trends. This chart of gate count versus feature size shows the ranges of silicon efficiency for the three approaches to application-specific ICs. Minimum feature sizes are coming down for all three approaches.

An apostle of silicon compilation

John Gray has a mission. He is busy spreading a gospel which, as he sees it, will eventually be accepted and overturn existing methodologies for microcircuit design, cut drudgery and time, and produce first-time-right very large-scale integrated-circuit designs.

He is one of the elite band of California Institute of Technology alumni who, in a short but prolific period in the late 1970s and early 1980s, developed the ground rules for structured VLSI design and coined the term silicon compiler. To translate these ideas into commercial products, he cofounded Lattice Logic Ltd. with Irene Buchanan, in Edinburgh, Scotland, in 1982, and that same year announced the world's first commercially available silicon compiler for random logic.



After receiving a PhD in computer science at Edinburgh University, Gray, who was born in Newcastle-on-Tyne, England, moved to Caltech in 1979, where he directed an industry-funded silicon-structures project in Pasadena. During that period, Caltech's Carver Mead and Lynn Conway of Xerox Corp. produced their seminal work on structured design methods, *An Introduction to VLSI Design*, and David J. Johannsen developed Bristle Blocks, a silicon compiler for laying out the data path of a central processor unit.

Johannsen's work held out the possibility of laying out an IC in a matter of hours or days, instead of months and years. In 1981, Johannsen, Mead, and Edmund Cheng set up Silicon Compilers Inc. in Los Gatos, Calif. [*Electronics,* Oct. 20, 1983, p. 47]. Meanwhile, Gray returned to Scotland, and thus began a friendly rivalry between the two silicon compiler outfits.

Though the two spinoffs share a common design philosophy, their objectives are different. "Silicon Compilers Inc. set out to commercialize Bristle Blocks and they have done a fantastic job of it," says Gray with genuine admiration. But he adds, "Not everybody wants to design a data path for a microprocessor. Many more need to design custom circuits with lots of random logic." Gray set out to win customers over to structured design techniques by presenting his compiler software in a design format with which they were familiar.

In fact, Lattice Logic's silicon compiler, designated Chipsmith, is dressed up as an automatically routing gate-array system. The Chipsmith works by completing connections between rows of pre-diffused transistors and the wiring channels between each row. In addition, the software will generate a new gate-array structure automatically. As an alternative, a customer can take a full-custom route. The compilation software is similar in both cases, the only difference being that the unused transistors and wiring channels in the gate array are eliminated.

Industry reaction was skeptical at first [*Electronics,* July 28, 1982, p. 46] but by November 1983, Ferranti Semiconductors, a pioneering and hard-headed gate-array manufacturer in Oldham, Lancs., UK, announced that it had signed Lattice Logic to help develop a new family of autorouted gate arrays. And earlier this year, John Gray, who doubles as software designer, fund-raiser, and salesman, won a first U.S. beachhead: Lattice Logic was awarded a contract from VLSI Technology Inc., San Jose, Calif., to supply its silicon compiler, which VTI will redistribute as part of its compiled cell library.

For Gray, this is just a start. Now he wants to concentrate on the market for third-generation supermicrocomputer-based work stations, and on new product development, with particular emphasis on the development of silicon compilers for other design styles. **–Kevin Smith**

the application-specific IC area is the recent agreement among Texas Instruments, Signetics, and Philips to standardize cell libraries using the Electronic Design Interface Standard, and offering the resulting cell library data base in 27 worldwide design centers.

Increased government funding in the Very High-Speed Integrated Circuit Program and development of gallium arsenide technology promise to speed small chip geometries and high-speed circuits into production. Significant memories and logic parts have already been built in GaAs by GigaBit Logic, TI, and Fujitsu. In Japan, the GaAs technology is an important aspect of the supercomputer effort. U.S. users of GaAs such as Tektronix, Motorola, and TI have concentrated primarily on instrumentation and communication applications.

Meanwhile, the VHSIC partnering program is moving from research into preproduction testing for parts such as static random-access memory test vehicles. TI, for example, has succeeded in developing a number of chips in a GaAs gate array. Based on GaAlAs/GaAs heterojunction bipolar technology, the part contains 1,024 internal gates with 64 input/output pads in a 3.8-by-3.56-mm chip. Propagation delays are typically 1.5 ns/gate at 0.2 mW and 0.4 ns at 1.0 mW. The speeds are similar to those of emitter-coupled logic but at one fifth the power. Molecular beam epitaxy is used to grow the heterojunctions on 2-in. wafers with ion implants to control doping and planar isolation. ☐

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ATE COSTS ARE SWELLING AS CHIPS SHRINK

Testing fast, more complex VLSI chips drives costs up and forces critical decisions on expensive automatic test equipment ☐ *by Jon Turino*

The increasing use of large and very large-scale integrated circuits is driving testing's cost contribution up from traditional levels, between 5% and 10%, to as much as 45%—and even more in some cases. At the same time, the rapidly rising price of test equipment has hit more than $1 million for a single-chip test system. In 1984, to cope with the increased volume and complexity of these high-gate-count components and the products they populate, over $1 billion will be spent on automatic test equipment for chips and printed-circuit boards (Fig. 1). By 1988, the ATE market may be more than 2½ times greater than it was in 1983.

The capabilities, limitations, and cost of LSI and VLSI ATE for integrated circuits and pc-board assemblies are now having an impact on engineers and engineering managers. Product design functions are affected as designs are tailored for testability as well as for performance. Industrial engineering functions fall under the same influence as ATE becomes an integral part of the flow of material through factories.

Quality assurance and control have been confronted with the large amounts of information about defects and fault distributions that ATE can generate. Manufacturing managers can use ATE information to improve their operations. Finally, the large investment required for equipment, fixtures, and software means that top management must share in the responsibility for choosing ATE for LSI and VLSI ICs and pc boards.

Critical issues

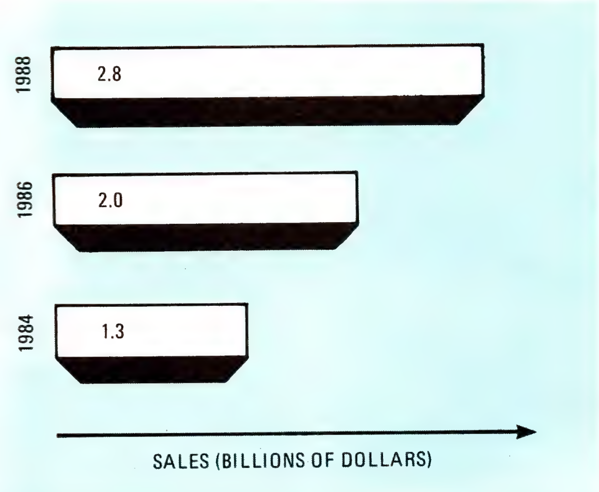
ATE is appropriate for LSI and VLSI when it can be used to test chips and pc boards containing ICs whose gate counts exceed 10,000 (LSI) or 100,000 (VLSI). Among the parts in these categories are 8-bit microprocessors—the 8088, the 6800, the Z80, and so on—usually referred to as LSI chips, and 16- and 32-bit microprocessors—the 80186, the 68000, the 32032, and the rest—usually described as VLSI chips.

ATE for LSI and VLSI parts and boards must cope not only with the microprocessors and microcomputers themselves but also with many support or peripheral chips. In many cases, they are even more complex than the processors and thus present even more difficult testing challenges.

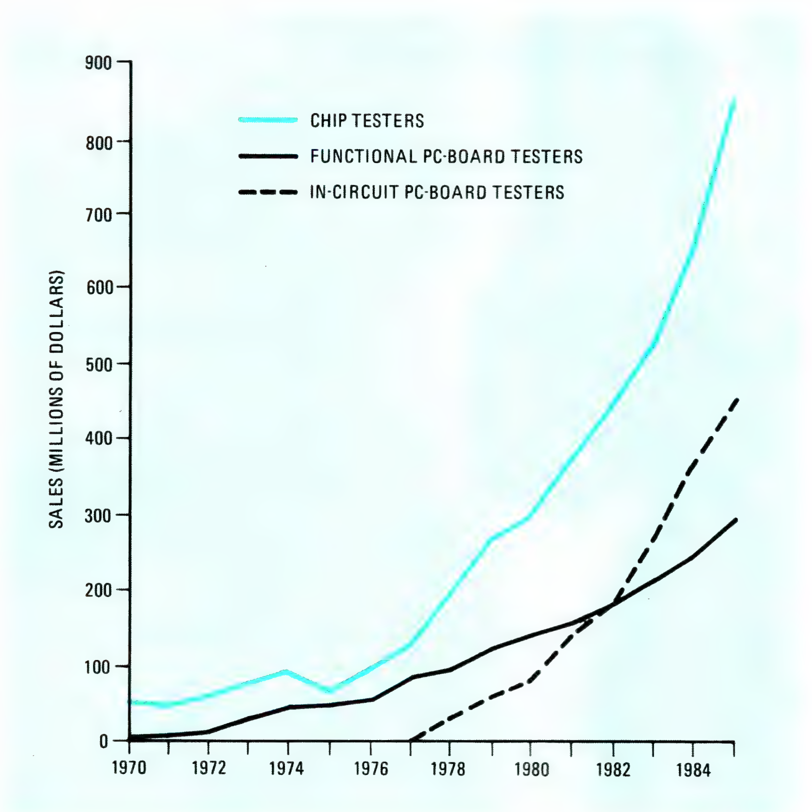
LSI and VLSI ATE has been segmented into two broad categories: IC testers and board testers. However, traditional definitions are starting to blur, because ATE for chips is sometimes used to test boards. Moreover, the parts under test are, in effect, boards that have been shrunk onto silicon.

LSI and VLSI ATE has been divided between two additional categories: benchtop systems and large systems. In general, benchtop equipment costs less than $250,000 and sits on a table or workbench; large-system ATE commonly costs $250,000 or more and is usually too large to mount on a surface. All large-system ATE stands alone on the factory floor, sometimes housed in its own controlled environment. The explosive growth of semiconductor ATE over the past 15 years, shown in Fig. 2, is predicted to account for a $1.3 billion market for 1984.

Several forces currently affect the selection, implementation, use, and support of LSI and VLSI ATE. They



1. ATE growth pains. Although automatic test equipment unit costs will decrease over the years, by 1988 higher unit shipments are expected almost to triple 1984 dollar sales, to $2.8 billion.



2. Sharp gains. Sales of commercial ATE equipment have mushroomed over the past 15 years, with device testers enjoying the hardiest growth as a result of semiconductor production demands.

include the shrinking of pc-board assemblies onto ¼-in. squares of silicon, the critical need to prevent defects in manufacturing, and the benefits to be gained from integrating ATE with computer-aided-design, -engineering, and -manufacturing systems.

Other factors include: increased chip and board complexity; the ever-higher speeds at which they operate; new packaging techniques at almost every level of assembly; the forcing of design-for-test disciplines into the engineering development environment; and the pressure on ATE vendors to halt the dramatic rise in the cost of LSI and VLSI ATE capital equipment and programming. The expense of LSI and VLSI IC and pc-board ATE has gone beyond the level that small- to medium-sized electronics manufacturers can afford—not just the expense of capital equipment but also of programming, fixturing, and support, which often runs far higher than the purchase price.

For all these reasons, users are exploring alternatives. Moreover, test-engineering professionals are becoming severely disenchanted with the need continually to duplicate certain mundane activities, such as entering circuit models and net lists into ATE, when they can be translated with relative ease from their CAD/CAE data bases into ATE language. Much attention is currently being paid to integrating CAD/CAE with ATE.

New packaging technologies, such as surface-mountable components, are beginning to appear in volume. In fact, one of the reasons for their failure to appear in force until now has been the hesitation of engineers who do not know how to test these pc boards with that old standby, the bed-of-nails tester (see "What is VLSI testing?" p. 73). These new packaging technologies can only be implemented effectively through design for testability and built-in test, the two most critical issues of the 1980s for LSI and VLSI ATE.

Only with these new test technologies will tomorrow's products be tested at today's prices. Increased complexity will not permit any rollback in testing costs, but these two methods will at least provide a measure of control. Top management's ignorance of—or unwillingness to admit—the huge profit opportunities created by the new techniques is still a problem.

The historical lag between ATE performance and unit-under-test requirements has been worsened by LSI and VLSI. At the chip level, the hardware is managing to keep up reasonably well, but software simulation systems based on small- and medium-scale IC architectures are slipping rapidly. At the loaded-board level, both hardware and software require revolutionary approaches—perhaps ATE-on-a-chip for hardware and new simulation techniques integrated with CAD systems in the software arena.

As the product shrinks, the ATE systems used to test it are growing. Chip manufacturers' demands for faster, more powerful, more accurate, and more sophisticated tests are making ATE physically larger just as floor space in semiconductor manufacturing facilities is becoming more expensive. A comparison of the size ratio between an ATE system and an IC under test is proof that ATE has not benefitted from the ability to pack more and more features and functions into smaller and denser packages.

Board test requirements have also been increasing with greater board size. ATE systems must be equipped with more pin electronics to handle higher node counts. Pin electronics has become more sophisticated to cope with the higher speed and longer test-pattern requirements brought about by LSI and VLSI. Board testers must now have the capabilities once required only in system testers. The reason is obvious: today's boards are the systems of yesterday. The next extension will be the shrinking of the system itself to the chip level.

Defect prevention

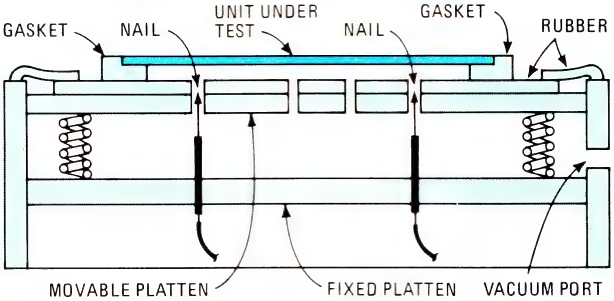
Semiconductor manufacturers learned very quickly that yield—the number of good devices they could get from a processed wafer—was the single most critical factor in the business. It does not matter how technologically superior the product is; if it cannot be delivered in quantity and at a profit, it is useless. Much of the testing that goes on in chip manufacturing is aimed less at verifying the performance of the parts than at finding out what, if anything, has happened to the process when test results indicate a change in chip characteristics, parameters, or yield.

ATE systems for LSI and VLSI have been tied into

What is VLSI ATE?

Automatic test equipment for very large-scale integrated circuits is controlled by mainframes, minicomputers, or personal computers. It is used to verify certain parameters of a unit under test and to identify and isolate defects that may be present on it.

At the system's heart is the control section, consisting of a computer, its peripherals, and its software. Under an operating system, the computer executes application-specific software that directs the system's stimulus, measurement, and switching resources to yield the desired test results and data. The measurement section evaluates the unit's response to directions from the stimulus section. The switching section acts as the programmable path network between the stimulus and measurement sections. The control section will then operate upon the information obtained from the measurement section and determine the next action to take.



Typical stimulus gear for LSI and VLSI and printed-circuit board ATE include power supplies, signal generators, and data driver pins, all programmable. Typical measurement gear includes digital multimeters, timer-counters, and data receiver pins. Switching systems may be constructed either of relays or solid-state logic circuits, depending on the levels and types of signals to be routed. The stimulus, measurement, and switching devices and circuitry can be configured as individual items interfaced to the control section's central processor or designed as integrated, multifunction electronics assemblies.

ATE for LSI and VLSI chips is designated as functional, parametric, or a combination of both. Within the parametric category, ATE may be further classified as dc or ac. Functional ATE exercises only the functions of the unit under test and does not make specific parametric measurements beyond those needed to determine whether or not the unit works. It does not normally provide actual data about the parameters it uses, because it does not normally contain measuring instruments that can ascertain them. Pass/fail limits are typically programmed into the system when the application test program is written.

Adding parametrics involves supplying enough hardware and software to provide actual measurements in engineering units—that is, volts, amperes, and seconds. Dc parametrics refers to such parameters as input current, output voltage, and supply current; ac parametrics includes such parameters as rise time, fall time, and propagation delay.

Functional ATE can provide a go/no-go indication of parameters without adding actual measurements in parametric units. For dc parametric approximations, one way this can be accomplished is to run the ATE with drive levels, thresholds, and loading conditions set as close as possible to the parametric limits of the unit under test. Some ac parametric approximations can be achieved by testing at a speed as close as possible to the unit's maximum and evaluating the response as soon as the ATE can capture it. For actual readouts in engineering units, a functional tester with parametic measurement capabilities is required.

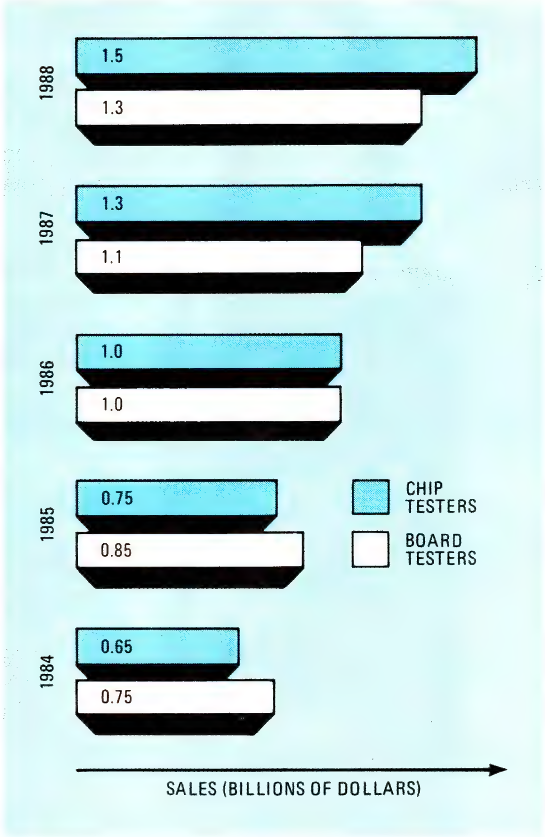
ATE for LSI and VLSI printed-circuit boards is most often designated as in-circuit or functional; the functional category is further divided between two others: static or dynamic. Static functional testing, carried on well below the speed of the unit under test, is not considered LSI- and VLSI-compatible. Dynamic testing occurs at the speed of the unit under test or as close to that speed as possible.

Functional testing is the process of accessing the normal input/output interface of the unit under test—that is, its edge connector pins—plus whatever special access may have been provided for testing. It also provides stimulus patterns and measurement verification that the unit works. This kind of testing relies on the assumption that if it does so, each component must be the correct one, all are installed correctly, and no process-induced problems exist. That assumption is generally correct.

In-circuit testing refers to the process of accessing all the nodes (electrical interconnections) on a pc board and sequentially verifying each component's parameters and limited functionality. It is based on the following reasoning: If every component is the correct one for its specific location, if all are installed correctly (that is, not placed upside down), and if there are no process-induced problems (for instance, solder short circuits caused by splashes), then it can be assumed that the board has been assembled correctly and will function. This assumption, too, is generally correct.

An in-circuit tester for LSI and VLSI pc boards usually has pin electronics (drivers and receivers) that can verify the functionality of each LSI and VLSI part it tests. It does not, however, check the ability of individual parts to function together with the others to which they may be connected. Nor does it attempt to verify timing parameters. Functional testers usually do both, at least to some extent.

The fixturing method used with in-circuit testers is called the "bed-of-nails" approach. A typical fixture (see figure) uses spring-loaded pins that touch the nodes of the unit under test when a mechanical, pneumatic, or vacuum stimulus is applied. Edge-connector fixturing is normally the method used with functional testers; however, it is practical to use a bed-of-nails fixture with a functional tester to provide increased visibility and control for testing and fault isolation. Some engineers distinguish between in-circuit and functional testers solely by the criterion of fixturing methods, but this distinction is incorrect. The real difference between in-circuit and functional testing lies in the type of testing performed.



3. Chip and board testing. Although 58% of all 1984 VLSI ATE has been earmarked for chip testers, with 42% allocated to their in-circuit and functional board counterparts, the ratio will be reversed by 1988.

sophisticated data-base management systems. Test results are analyzed, usually in real time, to ensure that defects are not allowed to creep into the manufacturing process. Silicon wafers are, at best, difficult to rework—and impossible in most cases.

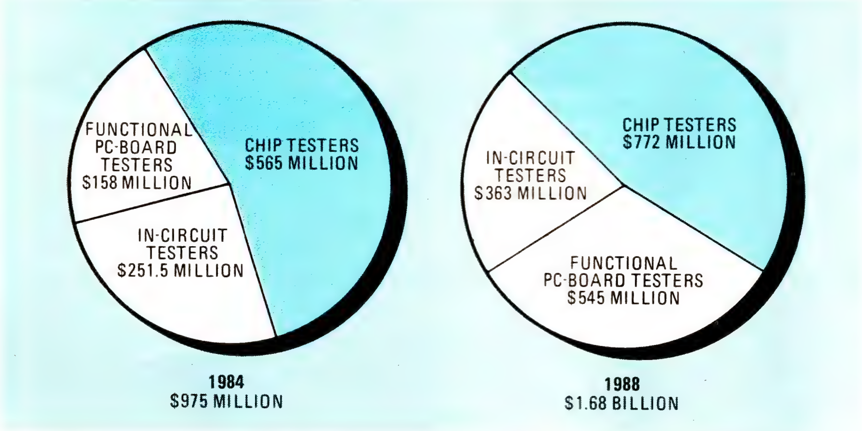
The users of LSI and VLSI chips have been slower to realize that the lowest testing costs are achieved when the fewest defects appear in parts manufactured. Perhaps one reason for the attention that efficient defect removal has received is that it is relatively easy, although somewhat expensive, to rework a pc board. The value added to most products has been large enough, and the demand great enough, to let pc-board manufacturers build in the profits needed to cover the high and sometimes invisible cost of this excessive reworking.

This state of affairs is changing as users of pc-board ATE begin to realize that for them as for device manufacturers, the greatest advantage lies in preventing defects, not in finding them. That strategy is so critical that quality circles and similar programs, long used in Japan, have for the past five years been adopted as valuable tools for improving the manufacturing process and reducing the costs of troubleshooting, reworking, and retesting. Thus LSI and VLSI ATE for pc boards is beginning to take on the communications and data-base management attributes of chip ATE, and users of the former are beginning to use the data-logging and -analysis functions now available.

Test professionals, though still concerned about such traditional ATE specifications as speed, accuracy, and resolution, are starting to focus on ATE as a tool to improve the manufacturing process. No longer are test engineers trying to verify electrical parameters at the loaded-pc-board level; they want to know if the board has been manufactured properly.

At the same time, new packaging methods are putting severe strains on current fixturing technologies. In addition, new ICs tend to operate at high speed, which makes traditional bed-of-nails fixtures less than optimal. Functional testers will therefore be used increasingly at a task for which they are not very efficient: fault isolation or removal. To bring functional testing costs down, the focus must shift to the prevention of defects, and the tester must be permitted to do what it does best: verifying the performance of the unit under test.

The worldwide market for LSI and VLSI ATE is expected to be about $1.3 billion in 1984 and to grow to about $2.8 billion by 1988. Growth will be slightly higher—in terms of dollar volume, not necessarily of units—for board testers than for device testers (Fig. 3). The current 1984 forecast suggests that 58% of all LSI and VLSI ATE dollars will be spent for parts testing, with the remaining 42% going to pc-board ATE vendors. By 1988, the ratio should shift to 46% and 54%, respectively. Currently, in-circuit testers make up the bulk of pc-board ATE shipments. The mix will change by 1988, when functional-tester sales will exceed sales volumes for in-circuit testers by a ratio of 1.5:1 (Fig. 4).



4. Functional and in-circuit testing. In 1984, U.S. in-circuit test sales will account for 26% of the VLSI ATE market, while functional board testing will account for an additional 16%. By 1988, the figures will be 22% and 32%, respectively.

Current worldwide ATE consumption (1984 forecast) is heaviest in the U.S., at 75%. Japan accounts for 15%, Europe for 9%, and the rest of the world for 1%. By 1988, the U.S. will probably account for only 60% of total world consumption, while Europe's share will grow to 15% and Japan's to 20%. Elsewhere, consumption will increase from the current 1% to about 5%.

Jon Turino is president of Logical Solutions Inc., a Campbell, Calif., consulting firm specializing in test-strategy planning.

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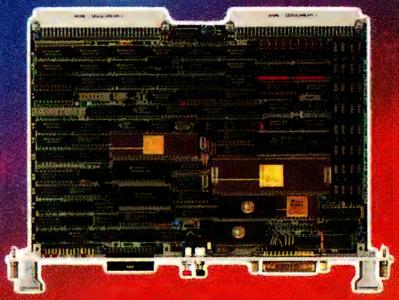

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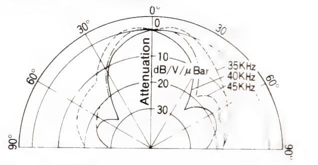
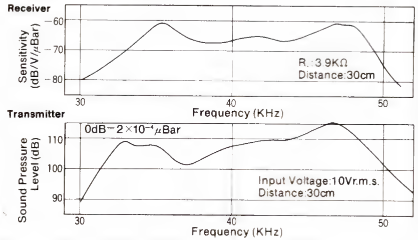


• Frequency Characteristics of MA40L4



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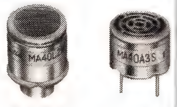

MA40L2 MA40A3

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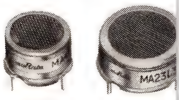

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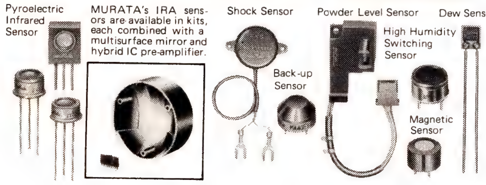

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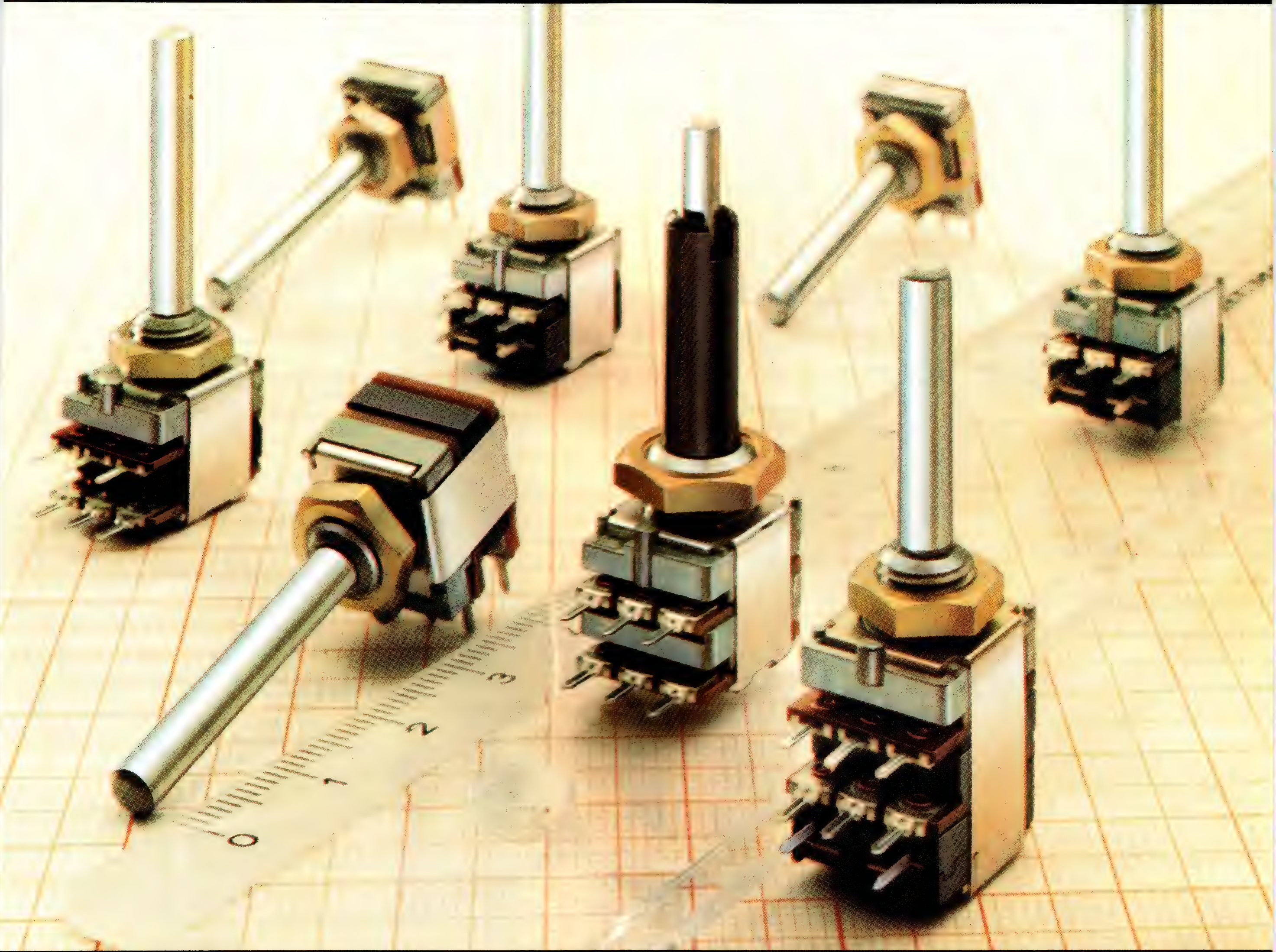

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  fiable en raison de sa technique de connexion non-vieillissante

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Comdex Oct.29-Nov. 1. 1984
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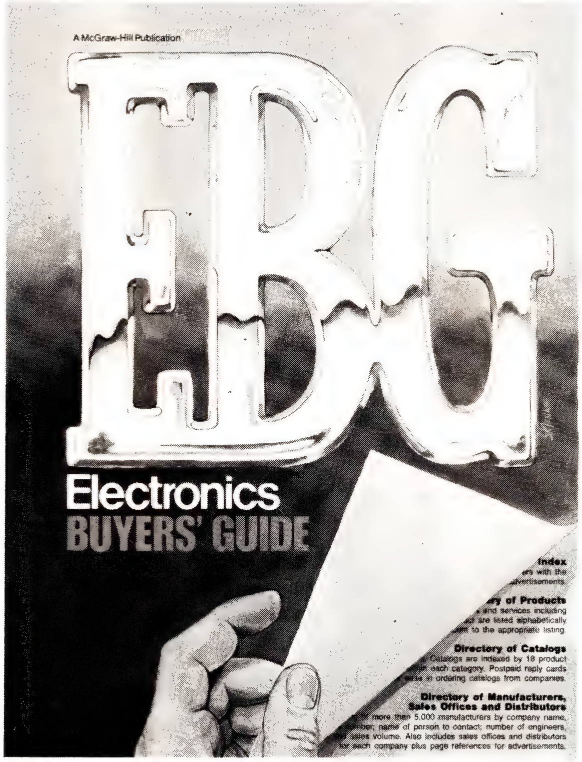
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- random conversion of level units dBm, dBµV, mV and µV

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- self-test

Signal Generator SMS 2

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NEW PRODUCTS

16-BIT CMOS CHIP REPLACES MANY OCTAL REGISTERS

Multilevel pipeline register with two sets of input/output instructions provides increased flexibility in digital signal processing ☐ *by Steve Zollo*

Billed as being as fast as—if not faster than—equivalent bipolar circuit combinations, a 16-bit CMOS pipeline register from Logic Devices Inc. replaces eight octal registers or two 8-bit pipeline registers in array processing and systolic array designs. The LPR520 and the LPR521, a similar part, are 16-bit replacements for Advanced Micro Devices Inc.'s Am29520 and Am29521 8-bit registers.

The parts feature four 16-bit registers that can be operated as two independent two-level registers or as one four-level register; they operate at an access speed of 25 ns or less. Both are TTL-compatible.

In the implementation of most digital-signal-processing systems, registers provide the important elements of delay of staging for operations. The number of these needed to implement the delay function in TTL encroaches on valuable board space, however, and the power overhead may become excessive.

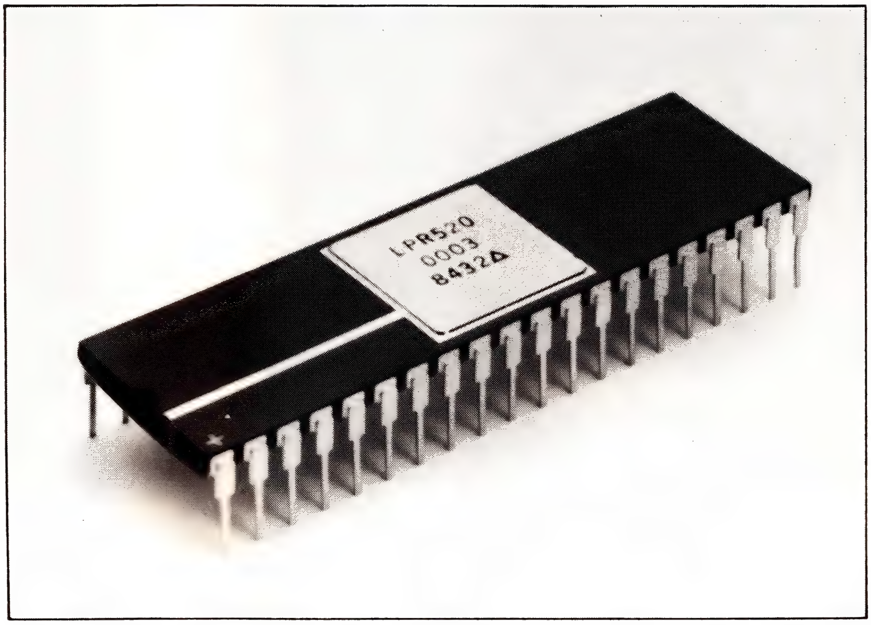
"By combining the capabilities of multiple devices in one chip, it saves valuable board space and it also offers the proven CMOS advantages of low operating temperature and low power demand," says Jamie S. Martorell, vice president of sales and marketing. The circuit's multilevel architecture is combined with two independent input/output instruction sets that permit data to be written to one register while it is being read from another register.

The two versions of the circuit differ only in the way they handle and preserve data between registers on a load instruction. The LPR520 shifts data through its registers as new data is received and overwrites data in the last register. The LPR521, on the other hand, retains data in subsequent registers and overwrites data stored in the first register.

This allows the use of the circuits as double buffers or ping-pong memory elements serving two processors. While one is writing data into the register, the other can simultaneously read an earlier result that has been moved into the second register bank. The register configuration of the circuits is determined by input instruction code, and data is latched into a register on the rising clock edge. All four registers in both parts are individually selectable at the output, and all outputs are three state and 16 bits wide.

The LPR520 and LPR521 can also be used as the delay element when two or more delays are required to synchronize microfields with data flowing through a pipeline architecture; it can also provide the reconfigurable delay or address staging required by exception conditions or branches in some pipeline circuit designs.

Multiple LPR520s or LPR521s can be cascaded to implement a filter requiring more delay than is available with a single circuit. Both parts are available in plastic or ceramic 40-pin dual in-line packages. In commercial-temperature-grade plastic, they sell for $20 each in lots of 100; in military-temperature-grade ceramic DIPs, the cir-



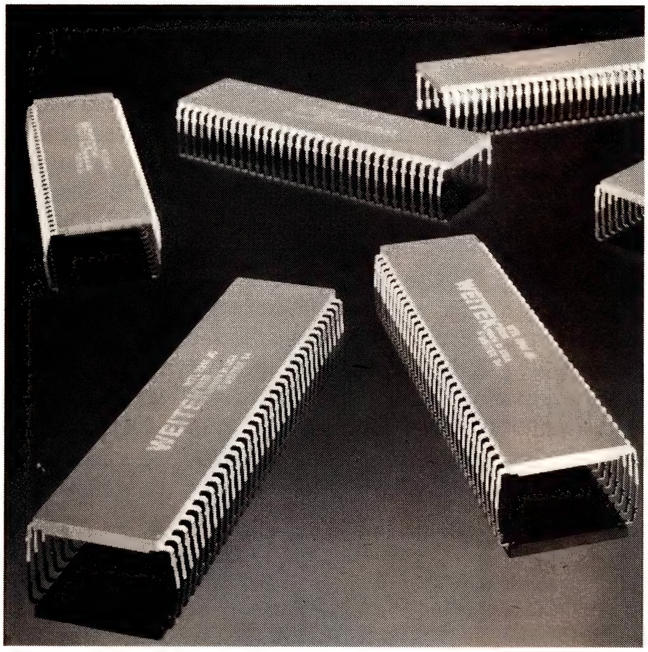
cuits sell for $64 each in like quantities. Samples are available now, with delivery or production quantities promised to begin in the fourth quarter.

Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, Calif. 94086.
Phone (408) 720-8630 [Circle reader service number 338]

Common algorithm helps circuit multiply in 35 ns

By sacrificing die size and using a common algorithm, Weitek has been able to come up with a family of 16-bit integer CMOS multipliers and multiplier-accumulators that work in as little as 35 ns (at 25°C). The products, which are targeted at signal-processing applications, range from a low-cost multiplier-accumulator without a preload function, the WTL 2044, through a set of pin-for-pin replacements for TRW's popular MPY parallel multiplier series and MAC multiplier-accumulator series, the models 2010 and 2516, respectively. Two multiprecision multiplier-accumulators, the 2244 and 2245, round out the line.

The 2244 and 2245 are expandable processors that can perform 16-bit, 32-bit, or 64-bit integer multiplication in any combination with full precision without having to use additional logic circuitry. This is achieved, the company claims, by the use of a Wallace tree and modified Booth encoding. In addition, the 2245 offers multiplexed outputs.



The 2244, which runs at 35 ns, can be applied in a variety of digital-signal-processing functions, including digital filtering and fast-Fourier-transform processing; the 2245 is designed to handle algorithms that are limited by the capabilities of 16-bit processors in such digital-signal-processing applications as radar, sonar, and graphics.

The 2044, which runs at 50 ns and dissipates 200 mW, is a suitable multiplier-accumulator when a preload function is not needed. It also performs subtraction and double-precision addition and multiplication.

All the chips, which are available in dual in-line packages, pin grid arrays, or leadless chip carriers, are manufactured in 3-μm CMOS with an 8-μm metal pitch. Prices range from $165 each for the 2044 to $270 each for the 2245 when ordered in lots of 100 pieces. The parts will be available in November.

Weitek, 501 Mercury Dr., Sunnyvale, Calif. 94086.
Phone (408) 738-8400 [Circle 377]

Product Term Sharing allows routing to chosen output pin

Four 24-pin programmable array logic chips have had their versatility increased by the addition of Product Term Sharing (patent pending), a feature that lets the designer share 16 product terms in any ratio between two outputs. This is accomplished by means of an architecture that allows a given product term to be routed to one of two output pins.

The PAL20RS series also offers programmable output polarity for active-high or active-low implementation and register preload, which allows function testing after programming. The chips operate at 20-MHz minimum and have a guaranteed propagation delay of 35 ns. Output drive is 24 mA with a 17-ns clock-to-output delay. Applications for the chips include discrete logic replacement, decoding, direct memory access, and data encryption/decryption.

The PAL20RS series comes in both plastic and ceramic 24-pin Skinny dual in-line package castings. Each chip sells for $23.78 when purchased in 100-lot quantities. Delivery takes up to 20 weeks.

Monolithic Memories Inc., 2175 Mission College Blvd., Santa Clara, Calif. 95050. Phone (408) 970-9700 [Circle 340]

Uses of wide-band amplifier cover radar to tomography

An integrated circuit with a 3-dB bandwidth of over 30 MHz, the XR-7000 log video amplifier has seven separate logarithmic elements as well as on-board voltage regulators in a single 40-pin package. This IC is intended for receiver and radar subsystems, spectrum analyzers, test equipment, ultrasonic imaging, and such medical applications as tomography.

In wide-range applications, all seven elements may be cascaded for a dynamic range of up to 105 dB. The elements' differential output currents are summed in a common base stage that has a maximum rise time of 17.5 ns with 100-Ω resistors.

A typical system with an input-signal change of 10 mV (80 dB) would change its output voltage by approximately 350 mV within 20 ns. In a dc-coupled crystal video receiver, the XR-7000 allows an overall dynamic range of 50 dB to be obtained at minimum cost, according to the manufacturer.

In the full-military version, the unit price of the XR-

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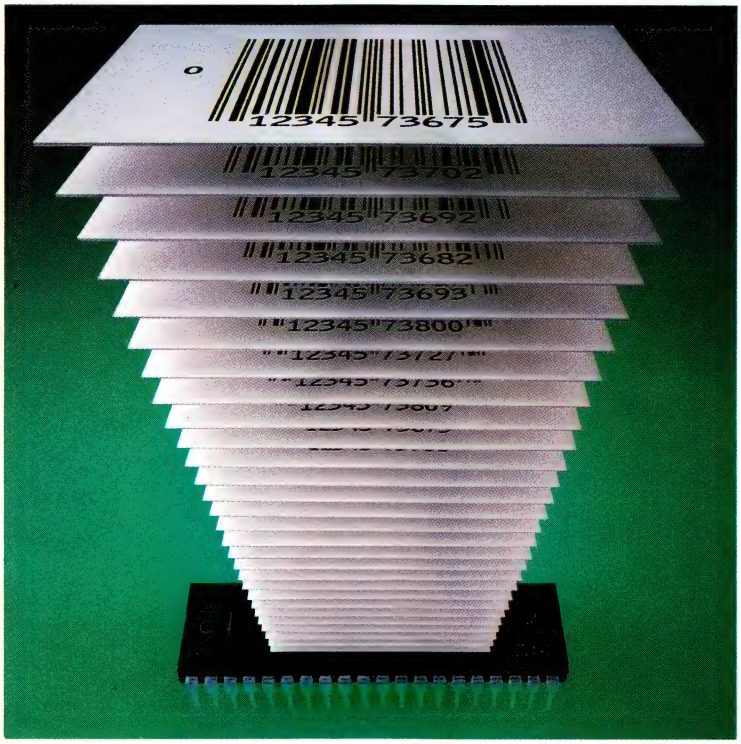
Now, designing in bar code capability is fast and easy with HP's new decoder IC and wands.



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HP's two new digital wands are designed for high performance bar code scanning in both industrial and commercial applications. They feature tough, replaceable sapphire ball tips, rugged construction, a variety of resolutions and a standard digital TTL interface. Each wand can be used at scanning angles up to 45 degrees for improved reading performance.

For your heavy industrial and LOGMARS applications, select from the new HBCS-4000 series sealed metal wands.

And for commercial or light industrial uses, choose from the HBCS-2000 series polycarbonate-cased wands.

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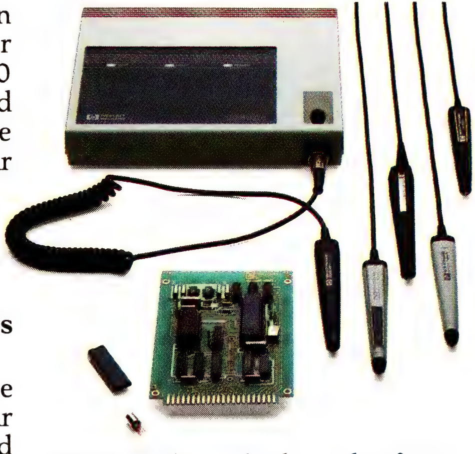

HP: The right choices for bar code solutions.

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For data and samples please contact:
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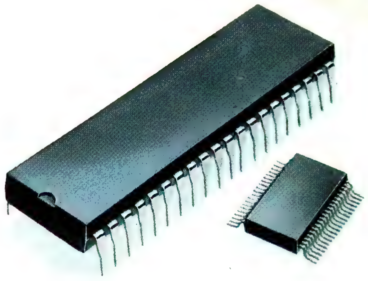

Philips put the PCxxx5 family and other ICs in space-saving SO mini packages. Comparison shown here is between 40-pin DIL and 40-pin SO.

Making the Most of CMOS

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7000 is $125 in lots of 100. Evaluation samples will be shipped in four to six weeks.

Exar Integrated Systems Inc., 750 Palomar Ave., Sunnyvale, Calif. 94086. Phone (408) 732-7970 [Circle 341]

Single-chip color processors have monitor, TV applications

A line of TV color processors and a color difference demodulator offers designers the entire PAL or NTSC color-processing function in a single integrated circuit, with a choice of features. Each of the parts contains complete color intermediate-frequency amplification with automatic color gain control, color killer, phase-locked oscillator, and color demodulators, as well as high-impedance dc controls.

The TDA3301/3303 red, green, and blue decoder chips are offered in 40-pin, 600-mil-wide plastic dual in-line packages. They have separate wideband red, green, and blue on-screen-display inputs that can be driven from either a character or a graphics generator to provide a display overlay on the composite signal. Automatic black-level setup dynamically adjusts the cathode-ray tube currents.

The TDA3330, housed in a 24-pin standard plastic DIP 300 mils wide, provides the full basic TV or monitor chroma system at low cost. It lacks the provisions for color overlay and automatic black-level setup.

The TDA3333 economically satisfies requirements for a color-difference format by taking the composite chroma portion of a PAL or NTSC and decoding it to R-Y and B-Y outputs. It is supplied in a standard-width 18-pin plastic DIP. In quantities of 100 to 999, the TDA3301/3303 sells for $5.14 each, the TDA3330 for $3.08, and the TDA3333 for $2.12. All are available now.

Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Ariz. 85036.

Pascal-2 compiler's programs run on many DEC computers

Operating on micro-, mini-, and superminicomputers from Digital Equipment Corp., a Pascal-2 compiler conforms to the International Pascal standard. Pascal-2 runs on the VAX with its VMS operating system, the PDP-11, and the Pro 350. It is also available for 68000-based Unix systems. Program-development tools include a high-level interactive debugger and an execution profiler.

Other utilities are program and text formatters, cross-referencers for program identifiers and procedures, a dynamic string package written in standard Pascal, and a set of definitions to allow Pascal-like use of macro code.

The manufacturer stresses that when the Pascal-2 compiler is used, programs developed on any DEC system can be carried over to all other DEC systems, with the source code remaining essentially intact. All versions of the compiler provide identical language features, with the same interface for the operating system and hardware and the same set of language extensions.

License fees for Pascal-2 VMS, available now, begin at $4,950.

Oregon Software Inc., 2340 S.W. Canyon Rd., Portland, Ore. 97201. Phone (503) 226-7760 [Circle 343]

C executive in ROM supports 1-megabyte address space

As a real-time monitor held in read-only memory, the C executive in release 1.5 supports the 1-megabyte physical address space of the 8086, 8088, and 80186 microprocessors. Support for C is built into the system, and a complete portable C library is included, containing over 100 routines for dynamic memory management, character string manipulation, ASCII-numeric conversion, and formatted input/output.

The C executive release 1.5 is packaged in both binary and source form. The binary version includes source code (in C) for various device drivers, and it may be used with several C compilers, including those from Computer Innovations, Lattice Logic, and Whitesmiths.

The executive is designed for minimum hardware configurations, the manufacturer states, and is aimed at the high-volume, low-cost board-lev-

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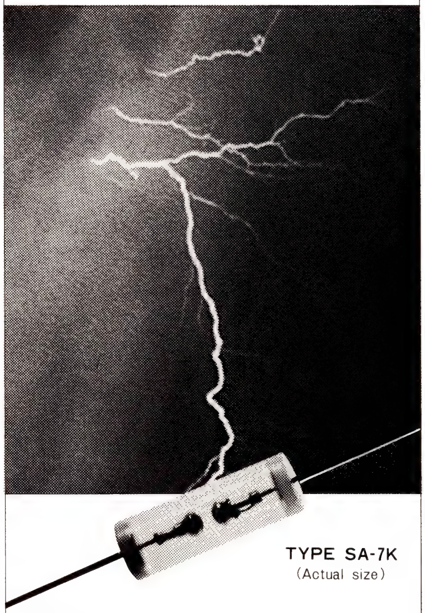

TYPE SA-7K
(Actual size)

● TYPE

Type	Breakdown Voltage (V) D	Insulation Resistance (Ω)	Maximum Surge Current (8×20us) KA	Life Times at 500A
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SA-200SS	200±10%	10^{19} min	1.0	1000
SA-80	80±10%	10^{10} min	1.5	3000
SA-140	140±10%	10^{10} min	1.5	3000
SA-200	200±10%	10^{10} min	1.5	3000
SA-250	250±10%	10^{10} min	1.5	3000
SA-300	300±10%	10^{10} min	1.5	3000
SA-7K	7000±1000V	10^{10} min	—	5000
SA-10K	10000±1000V	10^{10} min	—	5000
SA-180D(3)	180±10%	10^{10} min	2.5	10000

SA-180D(3) is a three electrode discharge tube.
All tubes can be made dark effect redused types which are available upon request. D is added to the model number, as in SA-80DSS.

● POINT

(1)Usable at wider ambient condition, especially good under high humidity.
(2)Visibility for operation.
(3)Compact and easy assembly.
(4)Stable characteristics.

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TYPE SA-80SS
(Actual size)

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MINIATURE: BLACK-LIGHT, UV-LIGHT,
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el market. Multiple C or Pascal tasks can run concurrently with intertask communication, resource coordination, and formatted input/output.

Multiple-user terminals, if needed, can be supported with Unix-like characteristics. Also included are real-time clock support, time-based task initiation, and other features for real-time applications.

Originally delivered for the 68000 and the Digital Equipment Corp. LSI-11, the C executive also supports the 8080, 8085 and 8086, 8088, 80186, the Z80, the 6809, and the 32000 series.

Delivery is beginning now of the C executive 1.5. Single-unit binary price is $500, plus $75 for documentation and media. Quantity discounts are available.

JMI Software Consultants Inc., 904 Sheble Lane, P.O. Box 481, Spring House, Pa. 19477. Phone (215) 628-0846 [Circle 344]

IBM's Fortran release 4 offers word-expansion option

Real-data precision is enhanced by the word-expansion option of VS Fortran release 4, the manufacturer says. In this release, 64-bit words can be expanded to 128 bits, through the automatic-precision-increase option, so that users do not have to recode their programs. It is also said to reduce programming effort when bringing Fortran programs from non-IBM machines to the IBM System/370, 4300, Personal Computer XT/370, or the 30XX family of processors.

In addition, it can access information directly by keyed data as well as sequentially or by record number; it also has the potential for multiple users to share a program in memory without having to load copies of the same program in each user's virtual storage.

VS Fortran release 4 runs under VM/SP, VM/PC, MVS/SP, MVS/XA, and VSE/AF operating-system environments. Most library routines are allowed to reside above the 16-megabyte line when used on systems running MVS/XA.

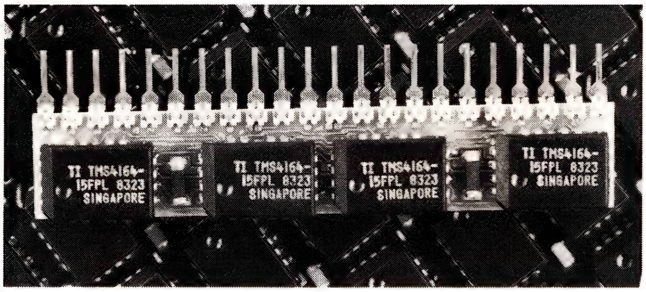
The manufacturer offers performance and usability enhancements that include enhance compiler options, compiler-listing output enhancements, in-line code generation for character assignments and comparisons, and out-of-line parameter lists for library input/output requests.

The basic license for the compiler and library for the System/370 is $699; the library is available by itself for $207. The program is available now.

IBM Corp., 900 King St., Rye Brook, N.Y. 10573.
Phone (914) 934-4000 [Circle 345]

Memory density increased by single in-line package use

High-density dynamic random-access memory modules organized as a single in-line package give more than 3.5 times as much memory in the same board area as conventional dual in-line package DRAMs, says the manufacturer of three SIPs, organized as 64-K by 4 bits, 64-K by 8 bits, and 64-K by 9 bits. This line of SIPs allows the designer the choice of adding memory to the same area or reducing the board area and thus the size of the sytem.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TI TMS4164-15FPL 8323 SINGAPORE
TI TMS4164-15FPL 8323 SINGAPORE
TI TMS4164-15FPL 8323 SINGAPORE

The 64-K-by-4-bit model is for mainframe and superminicomputer use, or wherever the physical size of the system depends on memory-system size. The models with 64-K-by-8-bit and 64-K-by-9-bit memory blocks are suitable for byte-wide applications using parity checking—for example, transportable systems, line-powered systems, and systems with large memory banks.

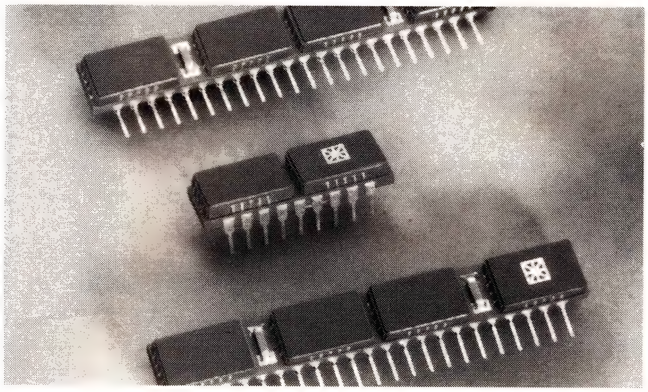
These three models are the first members of a family of compatible SIP modules to be built using DRAMs in plastic leaded chip carriers. The combination of plastic chip carriers with the board substrate reduces cost of the system from earlier implementations using ceramic components. All three SIPs are available with 120-, 150-, or 200-ns access times. In 100-piece quantities, the TM4164EC4-15 sells for $41.25, the TM4164FL8-15 for $82.50, and the TM4164FL9-15 for $87.50.

Texas Instruments Semiconductor Group, Literature Response Center (SC-451), P.O. Box 809066, Dallas, Texas 75380 [Circle 346]

Pin-compatibility choices give memory flexibility

A memory module that uses two industry-standard 256-K dynamic read-only memory chips, the EDH41512, is suitable for applications where a large amount of memory is needed in a small space. The module is pin-compatible with the same manufacturer's 128-K memory dual in-line packages (EDH4128 and EDH4264).

Also offered are the EDH411M and EDH44256, each of which yields 1 Mb of memory. The 411M and the 44256 are said to provide a density improvement of 4:1 over 256-K monolithic DIPs. Both single in-line pack-



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CIRCLE NUMBER 125

For more information, call the AMP Metrimate Desk at (717) 780-4400. AMP Incorporated, Harrisburg, PA 17105

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ages include two 0.22-μF decoupling capacitors.

The 411M, 44256, and 41512 are available with access times of 120 ns (230-ns cycle) and 150 ns (260-ns cycle). All three are available with MIL-STD-883 level B equivalent processing and in nibble-mode versions.

The 41512 is available in an 18-pin DIP utilizing two 256-K DRAMs in a leadless chip carrier mounted on a ceramic substrate. The 411M and 44256 consist of four industry-standard 256-K DRAMs in a leadless chip carrier on a 22-pin SIP ceramic substrate.

In 5,000-piece lots, the 150-ns versions of the 411M and the 44256 sell for $178.50. The price of the 41512, either the 120-ns or 150-ns version, is $89.25 in the same quantities. The modules are currently available.

Electronic Designs Inc., 35 South St., Hopkinton, Mass. 01748. Phone (617) 435-9077 [Circle 347]

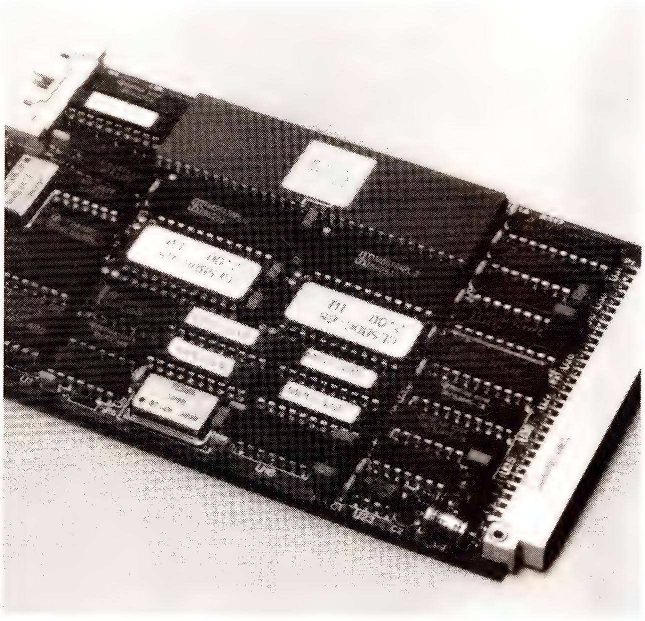
Low-priced board contains a 68000

Priced below $500, the Gesmpu-4A board incorporates a 68000 16-bit microprocessor operating at an 8-MHz clock rate. The Gesmpu-4A is on a standard single-height Euroboard (100 by 160 mm) and is compatible with the standard G-64 bus.

Four JEDEC (Joint Electron Device Engineering Council) sockets accommodate up to 128-K bytes of erasable programmable read-only memory and up to 16-K bytes of static random-access memory. The board also has a triple 16-bit timer and an RS-232-C serial interface with programmable baud rate.

The Gesmpu-4A can interface with a number of 8- and 16-bit compatible memories and peripherals that are also G-64 compatible. The manufacturer recommends applications in process control as well as in high-end microcomputers.

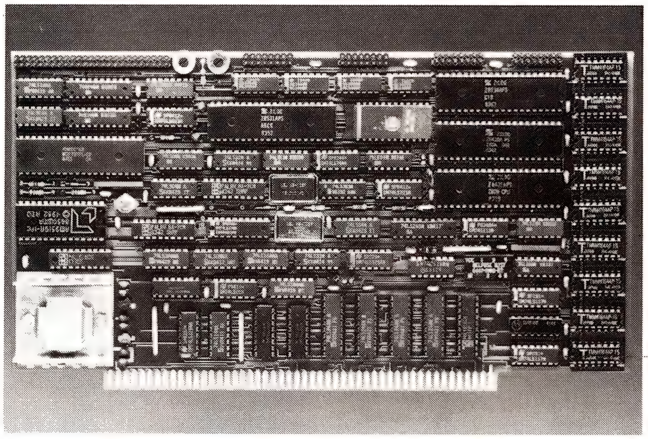
This product is supported with Gespac software, and 68000 debugger firmware is available for in-circuit debugging or evaluation of the board. Two disk-operating systems (CP/M 68K and OS-9) are offered, plus several utilities, assemblers, and compilers.



The unit price of the Gesmpu-4A is $475, and it is available now.

Gespac Inc., 550 E. Grandview, Mesa, Ariz. 85203. Phone (602) 962-5559 [Circle 348]

Z80B-based board serves needs of S-100 bus



With 128-K bytes of parity-checked random-access memory divided into two 64-K-byte banks, the Systemaster II, an S-100 master single-board computer, provides a transient program area from 60- to over 63-K bytes. A Z80B central processing unit or optional Z80H running at 8 MHz is recommended by the manufacturer.

Two RS-232-C serial ports provide either synchronous or asynchronous communications with software-programmable baud rates. The two 8-bit Centronics-compatible parallel ports may be combined to provide a 16-bit port, modified to provide a Small Computer Systems Interface, or, with an optional adaptor, configured to provide an IEEE-488 interface.

Simultaneous control of up to four 5¼- or 8-in. floppy disks is possible. The system will boot from either a floppy or a hard disk. Deliveries of the Systemaster II will begin Nov. 1, 1984. In original-equipment manufacturer quantities, the price will be $679.50.

Teletek, 4600 Pell Dr., Sacramento, Calif. 95838. Phone (916) 920-4600 [Circle 349]

Robot meets standards for class 10 clean room

Based on the firm's standard model A-O robot, the model S-110R is designed for manufacturers using contamination-sensitive materials. The robot meets class 10 clean room standards for its entire work envelope, eliminating contamination caused by human handling.

Called the White Robot, the system can assemble disk media over a spindle with a 0.0005-in. clearance between the disk inside diameter and the spindle outside diameter. The robot can also locate and radially orient the spindle

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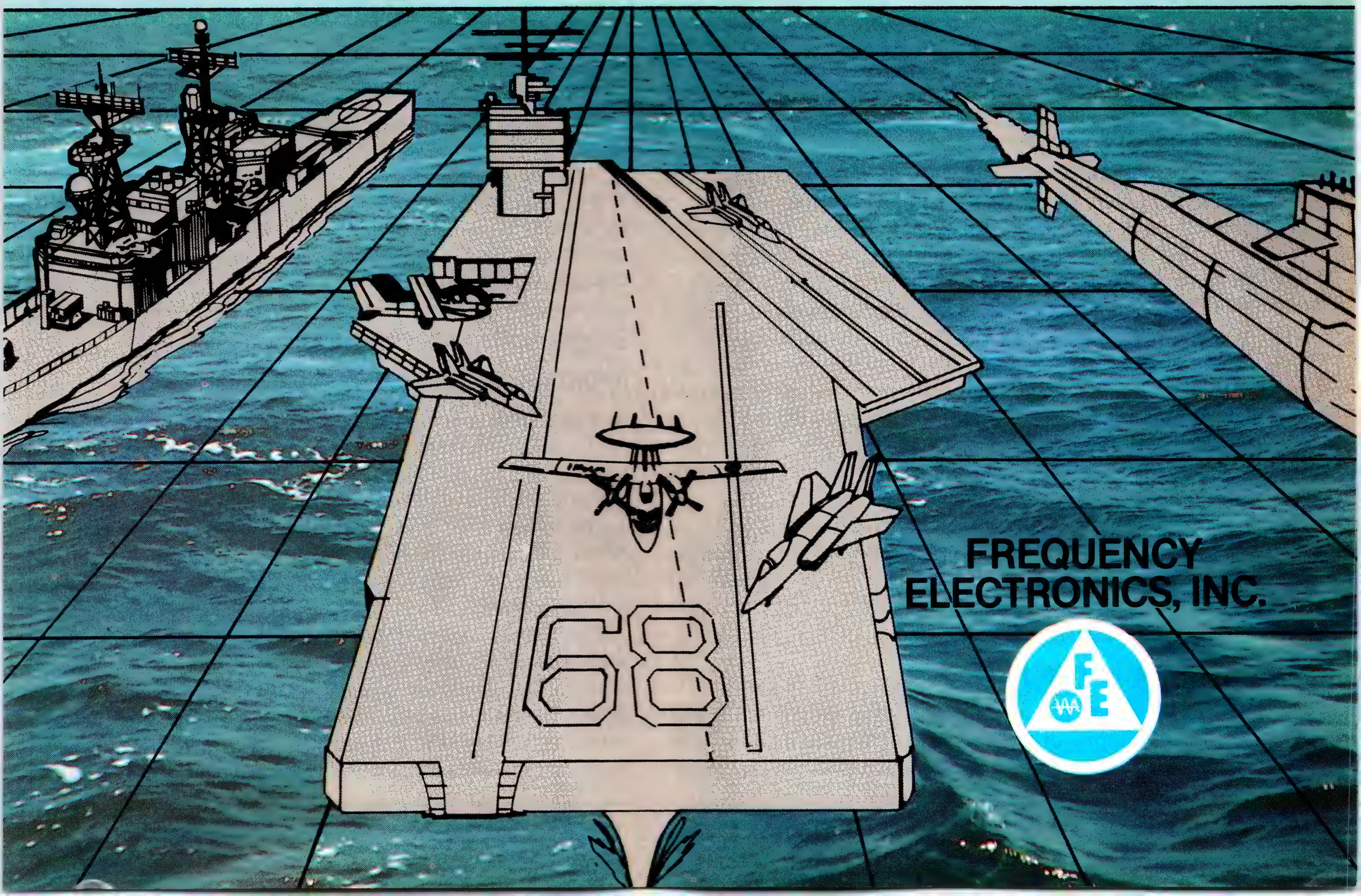
Circle 89 on reader service card



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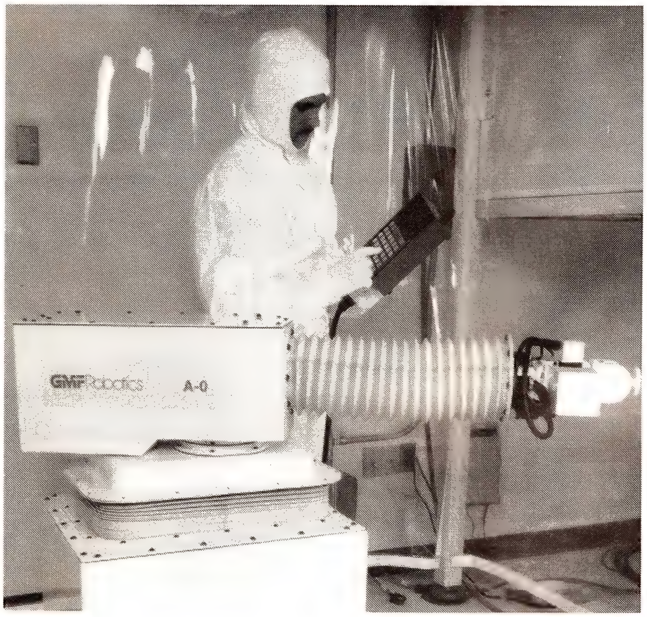


hub using a fiber-optic vision system, as well as gauge disk spindle height and runout to an accuracy of ±0.0001 in.

The price for the A-O model ranges from $35,000 to $55,000 depending on whether it's a Class 10 or Class 100 clean room model and the type of hand tooling chosen. The White Robot is available now.

GMF Robotics Corp., Northfield Hills Corporate Center, 5600 New King St., Troy, Mich. 48098. Phone (313) 641-4242 [Circle 350]

In-circuit tester sells for $2,495

A high-speed, easy-to-operate in-circuit test system automatically checks printed-circuit boards and integrated circuits without applied power or documentation. The ATS Searcher requires no special training—digital or analog pc boards or ICs are tested by visually comparing the nodal impedance signatures of chips suspected of having faults with versions that are known to be good.

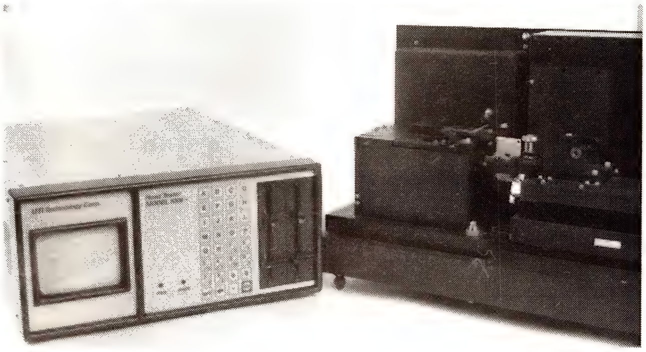
Capable of checking as many as 80 pins, the portable system tests in one fifth the time of manual probing, the company says. Simultaneously scanning pins while displaying signatures and pin numbers, the tester operates at from 18 to 120 V peak-to-peak open-circuit impedances. Accurate to ±5% on all ranges, the remote-controlled 10.5-lb system couples to board connectors and clips to ICs.

Available now, the ATS Searcher sells for $2,495.

Associated Technical Services, 212 S. Main St., Middleton, Mass. 01949. Phone (617) 774-6556 [Circle 351]

Floppy-drive head tester operates in two modes

Operating in its production mode, the model MTI/1000 automated floppy-disk-drive head tester automatically executes a predetermined test sequence and checks results



against pass/fail limits. The results of each test are shown by lighted pass or fail indicators. With interchangeable head and media adapters, the tester can accommodate flexures, buttons, or carriages on the available media.

In its engineering mode, the head tester permits the operator to select track, current, read load, and write frequency tests individually, and operate under computer control. The user has access to the tests and their set-up parameters as required. The engineering mode can also be used to set up items such as calibration factors and pass/fail limits.

The MTI/1000 uses a 2-in.-thick cast tool plate that is virtually impervious to deflections in order to eliminate mechanical vibrations and distortions that affect accuracy. The long-life spindle is held to tolerances several times tighter than those provided by drive manufacturers, the company says. Also, the ground leadscrew can position the head any place on the recording surface to a resolution of 139 μin.

The unit's testing electronics use a temperature-stabilized 12-bit analog-to-digital converter, gain-switching amplifiers, and several precision-controlled filter networks. Together, these are claimed to yield at least 90 dB of resolution.

Priced at about $28,000, the unit is available within 75 days from receipt of order.

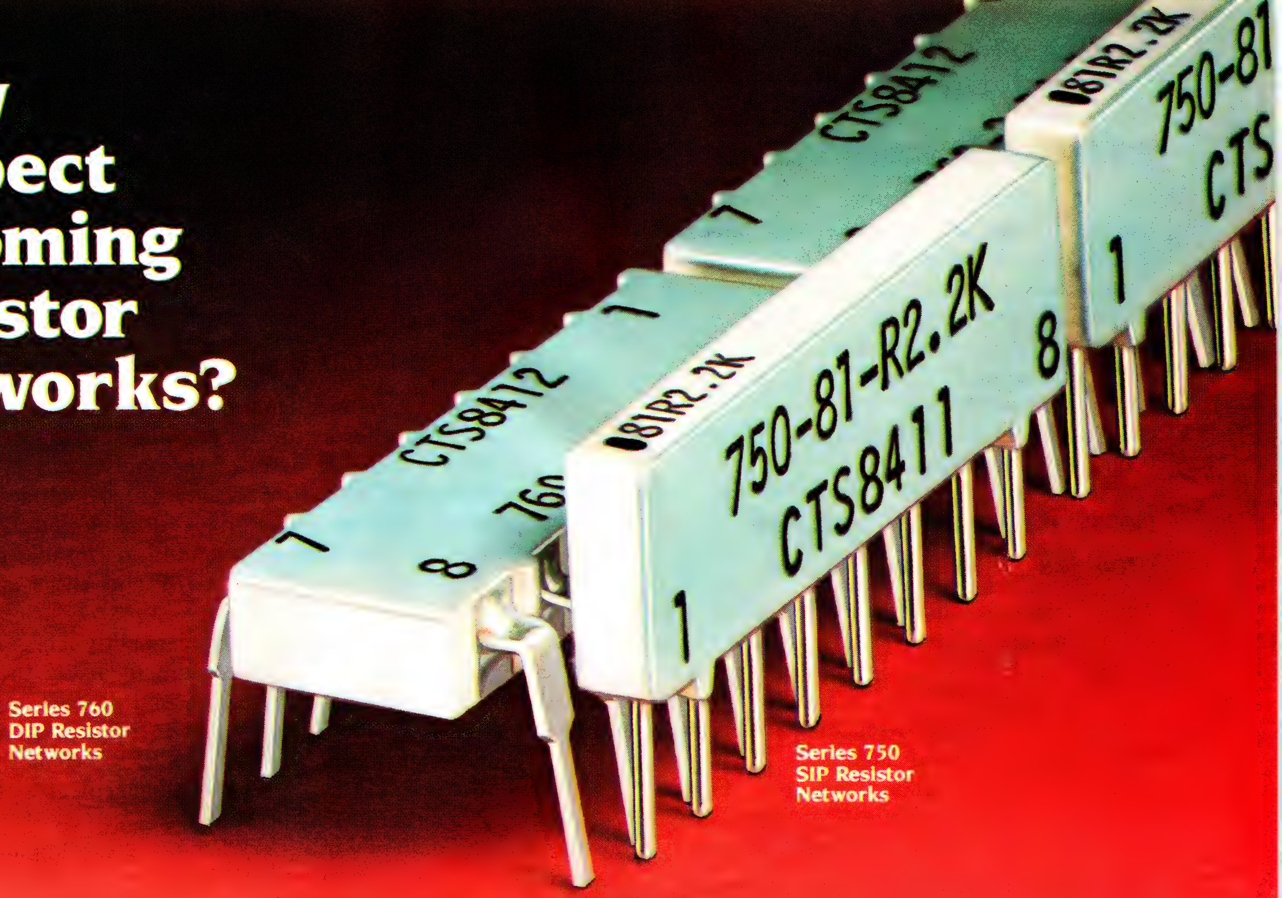
MTI Technology Corp., 6385 Rose La., Carpinteria, Calif. Phone (805) 684-6676 [Circle 352]

Single unit performs both in-circuit, functional tests

A single unit performing in-circuit and functional test operations, the Dual Level Vacuum Test Fixture is engineered for analog, digital, IEEE-488-bus, and power-supply applications. Because dual-level fixturing minimizes, or, in some cases, eliminates probe interference, printed-circuit boards requiring further testing or calibration at a black box tester can now be tested entirely by automatic test equipment.

The fixture incorporates two different interchangeable long and short travel probes to facilitate two-function testing. Designed for loaded board testing, the fixture lowers the unit under test and engages all pins for the in-circuit test. Then the fixture is brought to a higher level, maintaining contact with only the pins required for the

Why inspect incoming resistor networks?



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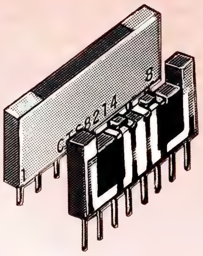

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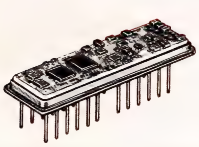

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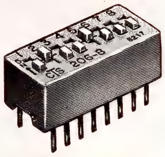

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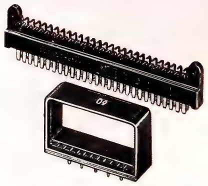

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functional test. The fixture increases test accuracy by eliminating the effects of unused pins, such as noise, antenna effect, capacitance, and resistance.

In addition, the fixture offers independent sequencing as well as receptacles and interfaces to many other testers; its probes are easily replaceable.

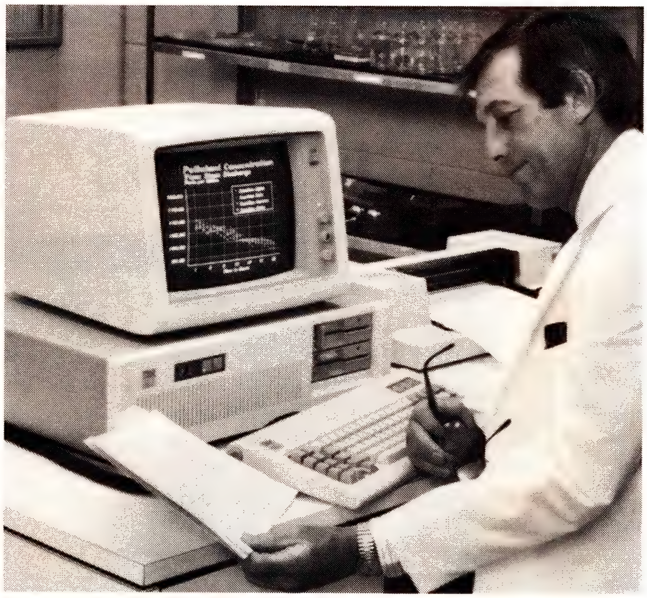
Prices start at $275, and the fixture can be delivered in six to eight weeks.

O-B Test Group Inc., 487 Jefferson Blvd., Warwick, R.I. 02886. Phone (401) 739-7310 [Circle 353]

Hardware, software enhance graphics abilities of PC line

The graphics capabilities of IBM Corp.'s personal computer line have been enhanced with a new series of hardware and software options for engineering and scientific use. The Personal Computer Engineering/Scientific Series assists engineers, scientists, researchers, and developers with specialized applications.

With the series, an IBM PC AT, XT, or PC with an expansion unit can create vivid color graphics, support engineering designs, control laboratory experiments, or perform high-speed mathematical computations, among other tasks. It includes the PC Professional Graphics Display and Controller, which can simultaneously display 256 colors from a palette of 4,096.



The PC Graphics Development Toolkit includes the Virtual Device Interface and other programs to assist in designing graphics and applications that are independent of such gear as displays, printers, and plotters. Also available are the PC Graphical File, Graphical Kernel, and Plotting systems, along with the Graphics Terminal Emulator, which help programmers develop high-performance graphics applications.

Available now for immediate delivery, the graphics display sells for $1,295, the controller for $2,995, the Toolkit for $350, the file system for $175, the kernel system for $295, and the plotting system for $225.

IBM Corp., Entry Systems Division, P.O. Box 1328, Boca Raton, Fla. 33432. Phone (305) 982-3328 [Circle 354]

Version of 8052 controller has on-chip Basic interpreter

A software-on-silicon version of the company's 8052 microcontroller features a complete Basic interpreter stored on chip in 8-K bytes of read-only memory. In addition, the MCS Basic-52 package, which includes the 8052AH chip, features full 8-digit floating-point arithmetic, a built-in capability to program an erasable programmable ROM and electrical EPROM, and a user-accessible function library.

The floating-point math capability lets complex control algorithms be calculated directly using the MCS Basic-52. The built-in EPROM and EEPROM programmer and a file-management system let a programmer write a program and save it on the EPROM or the EEPROM. Because of the chip's file-management structure, up to 225 programs to be stored.

The function library lets the user's application be written in the faster assembly language and use subroutines contained in EPROM or EEPROM if it cannot be executed with a Basic program because of speed considerations. The chip is suited for settings that require complex arithmetic control but where speed is not critical, such as temperature control and security.

The chip's Basic interpreter provides more features and 2½ times to 10 times higher-speed performance than Tiny Basic, the company says. Selling for $45 in quantities of 1,000, the 8052AH-Basic is available now for delivery.

Intel Corp., Literature Dept. L-17, 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (602) 961-2756 [Circle 355]

8-bit processor doubles RAM and ROM, keeps same code

With an 8-bit single-chip complementary-MOS microcomputer, users of the firm's model 80C48 and 80C49 can double or quadruple on-board random-access and read-only memory capacity without changing the instruction set. Designated the 80C50, the processor is upward op-code compatible with HMOS chips supplied by a number of manufacturers.

The chip offers the use of 111 instructions to ease the task of software development, while the competing HMOS device has only 98 instructions, the company says. Made with 3-μm CMOS technology, the 80C50 is a static RAM that has an operating frequency range from 0 to 6 MHz and a source-voltage-supply range of 2.5 to 6.0 V.

When operating at 6 MHz, the SRAM's voltage-supply range extends from 3.5 to 6.0 V. For the HMOS version, though, the voltage-supply range is 4.5 to 5.5 V at the same frequency. Designated the 80C40, a version of the processor without the on-board ROM is intended for use in prototype and preproduction phases of system

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To reach us, write: McDonnell Douglas Microelectronics Center, Applications Engineering, MO60/111, P.O. Box 516, St. Louis, MO 63166. Telephone (314) 234-8111.

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Circle 93 on reader service card

development. Samples of the 80C40 microprocessor are available now for a price of $11.50 each when they are purchased in lots of 100.

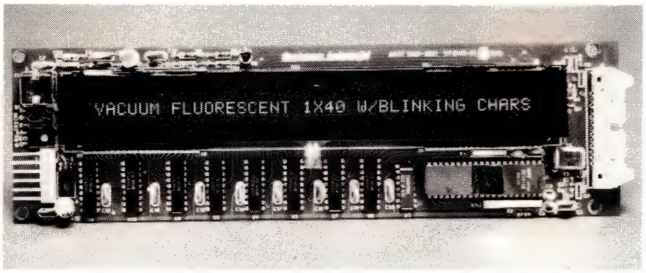
Orders of the 80C50 can be filled eight weeks after receiving the user's final ROM pattern; large production quantities take 16 weeks.

Oki Semiconductor, 650 N. Mary Ave., Sunnyvale, Calif. 94086. Phone (408) 720-1900 [Circle 356]

Fluorescent display adapts to most lighting conditions

A vacuum fluorescent display, the VF-0140-02, is a 1-line, 40-character (5-by-7 dot matrix characters) dot matrix display subsystem with blinking characters for applications requiring an operator-prompting capability. Also standard is a brightness control adaptable to most lighting environments. Full brightness readout is measured at approximately 200 fL. TTL parallel and serial data input are standard; RS-232-C is optional.

The VF-0140-02 is said to be a complete subsystem with an on-board microprocessor-controller for display-refresh and -control functions. The dc-to-dc converter generates the voltage required to drive and display. Hence, only a single +5-V dc power supply is required to operate the display. Power consumption is said to be 500 mA. The 5-by-7 dot matrix format allows generation of upper- and lower-case alphabetic characters and numerals, punctuation, and commonly used symbols that aid readability.



Priced at $164 in lots of 100, the VF-0140-02 is available for delivery now.

Beckman Industrial Corp., 2500 Harbor Blvd., Fullerton, Calif., 92634. Phone (714) 871-4848 [Circle 357]

A 16-line LCD has capacity of 128 by 480 addressable dots

Able to present graphics and alphanumerics in any combination, the F481C liquid-crystal display offers 128 by 480 fully addressable dots—two thirds as much display capacity as standard cathode-ray tube terminals, the company says. Power consumption is also said to be lower than that of a CRT. Suitable especially for portable computers, the F481C's 16-line display makes it practical for running spreadsheets.

Using a 5-by-7 format, the F481C can display 16 lines of 80 characters. To simplify interfacing with host systems, it incorporates all the drive and controls necessary to accept serial data and display it. The module does not contain a character generator, so designers can use any alphanumeric format that suits the application.

The module interfaces through eight input lines: power, ground, three clocks, a signal to begin the display scan, and two data inputs. The module also contains a power-conversion circuit that supplies the higher voltage needed for the LCD panel, making only one 5-V input supply necessary. Total power consumption equals 180 mW. Also, a temperature-compensation circuit adjusts the voltage received by the power converter to keep the panel's contrast at the right level over the F481C's temperature range of 0 to 50°C.

The compact F481C sells for $360 in quantities of 100 and is available from stock.

Seiko Instruments U.S.A. Inc., 2990 W. Lomita Blvd., Torrance, Calif. 90505. Phone (213) 530-8777 [Circle 358]

Array lets four LEDs be mounted on board at once

With a four-element array of light-emitting-diode indicators intended for printed-circuit-board mounting, users can mount four LEDs simultaneously. The 5640 series' black nylon housing block provides contrast with the LED colors and holds the indicators in alignment.

The LEDs are positioned on ¼-in. centers, and the overall length of the assembly is just 1 in. Leads have standard 0.1-in. spacing, and the assembly is designed so units can be stacked end to end if required. The indicator's housing includes board stand-off for easy flux removal after soldering.

Three off-the-shelf models are available with Super-Brite LEDs. In addition to the red, green, and yellow-colored models, the series is available with mixed colors, as well as with economy LEDs for use when highest brightness is not required.

Available now, the 5640E (with an economy LED) sells for $1.34 each in 1,000-unit quantities.

Industrial Devices Inc., Edgewater, N.J. 07020. Phone (201) 224-4700 [Circle 359]

VAX-based software system speeds pc-board design

The DNA2000 is a task-oriented software system designed for use with VAX mainframe computers. It automates the printed-circuit-board design process from schematic entry with phototools and manufacturing documentation, thus permitting VAX users to design pc boards faster. The software system has multiple autorouting routines, automatic schematic entry, circuit placement, and interactive design; checks the pc board for mechanical errors and electrical connections; and contains a selection of post-processing programs.

A distributed-process architecture allows the DNA-2000 software to be used without downloading the VAX processor. Interactive graphics performed by processors resident on the work stations won't disrupt tasks running simultaneously on the VAX. Available now, the

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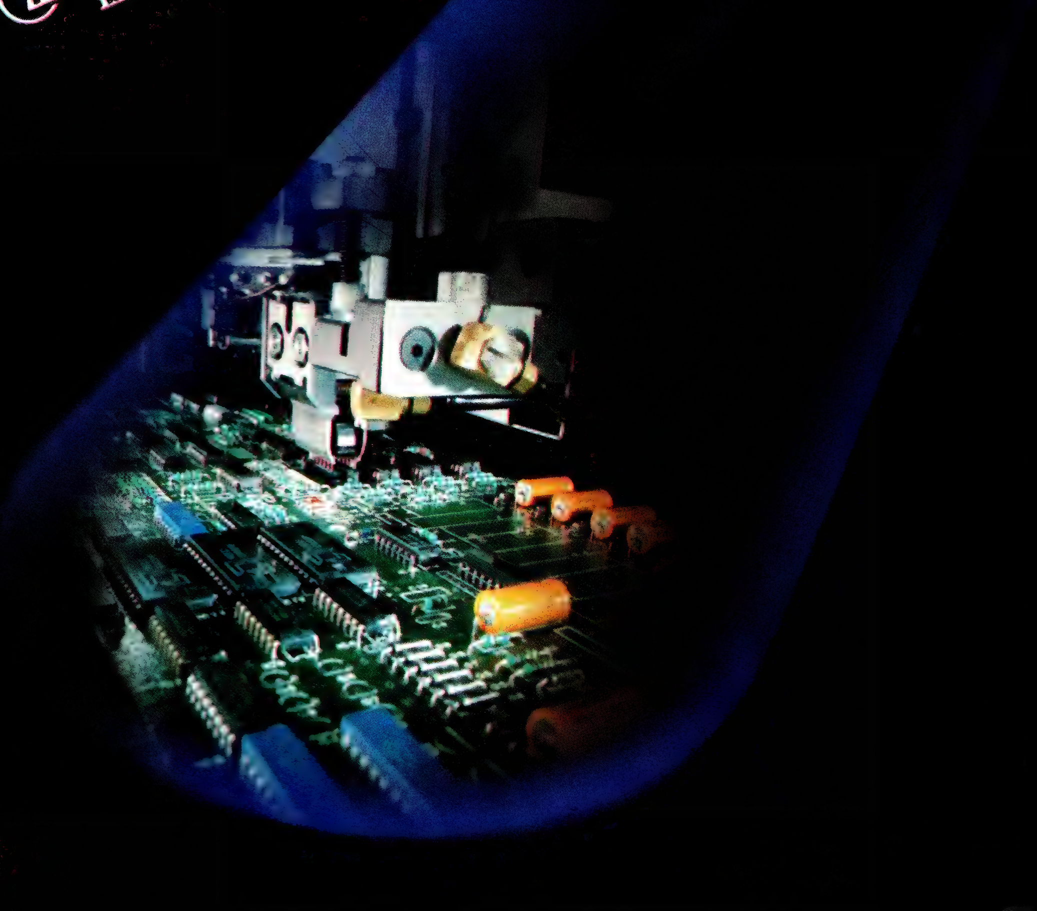


Circle 95 on reader service card

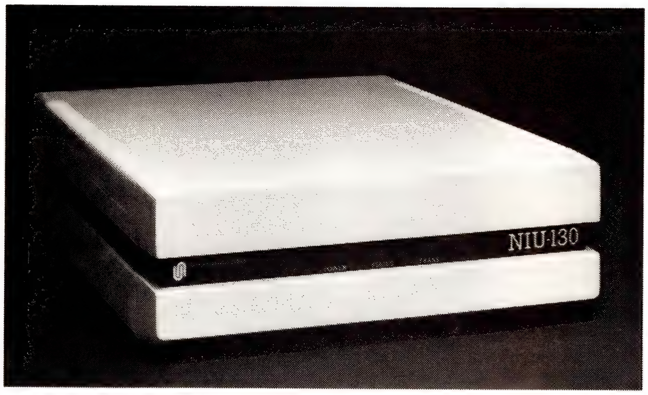
DNA2000 comes as bundled or unbundled software for user-tailored systems.

Prices start at $5,000 for schematic-capture software and increase depending on the number of other software options chosen. Interfaces to computer-aided design systems from other vendors are available, and the software also comes in a turnkey system for new VAX users.

Vectron Graphics Systems Inc., 2910 Corvin Dr., Santa Clara, Calif. 95051. Phone (408) 737-0460 [Circle 360]

Network interface connects two RS-232-C-based devices

With the NIU-130, two devices using RS-232-C interfaces can be connected to a Net/One local network at reduced cost, says the manufacturer. The interface provides the flexibility to interconnect widely separated terminals and printers and is supported by all four network media: broadband, baseband, optical fiber, and coaxial cable. The broadband model has an integral modem that transmits 5 Mb/s; all others operate at 10 Mb/s. All units execute network communications protocols in an Intel 80186 microprocessor with 128-K bytes of random-access memory. Said to be smaller than previous network interface units, the NIU-130 measures 3¼ by 9½ by 12½ in. Available in November, it is priced from $1,400.



Ungermann-Bass Inc., 2560 Mission College Blvd., Santa Clara, Calif., 95050. (408) 496-0111 [Circle 372]

Digital oscilloscope displays real-time, stored waveforms

The LBO-5825 is a 35-MHz, two-channel digital storage oscilloscope equipped with 2-K of memory, a 5-MHz maximum sampling rate, and pretrigger view capability. X-Y recorder output terminals are included for use with a plotter, and simultaneous display of real-time and stored waveforms are said to be possible. Also included are roll function, memory protect, external clock provision, and automatic chop/alternate model select.

The storage oscilloscope is said to be suited for stress analysis, shock and vibration testing, power-line transient monitoring, and computer-glitch problems. It may also be used for viewing events that occur infrequently.

The LBO-5825 can also be used for production-line environments since a stored reference waveform can be compared to an alignment waveform, thus speeding the final equipment adjustment. It is available for delivery now at a price of $3,850,

Leader Instrument Corp., 380 Oser Ave., Hauppauge, N.Y. 11788. (516) 231-6900 [Circle 371]

Pulse-dialing chip offers 17-digit memory

A pulse-generating integrated circuit, the MSM5249RS serves as the signaling interface between the keypad and a telephone network. It can be used with both single-contact and standard 2-of-7 keyboards.

The dialer incorporates a 17-digit redial memory that functions as a timing buffer for proper sequencing of the pulse output. The 17 digits stored in the memory can be redialed by pressing the * or # key.

Pulse signals are generated and timed by an internal resistor-capacitor oscillator operating with a minimum of external components. The signals produced can be set by hardware for either 10 or 20 pulses/s, and an audible tone output is available for key-press recognition.

Incorporating low-power complementary-MOS technology, the pulse dialer typically consumes 0.6 mW of power and can operate from a source of 2.5 to 6 V. It is supplied in an 18-pin plastic dual in-line package.

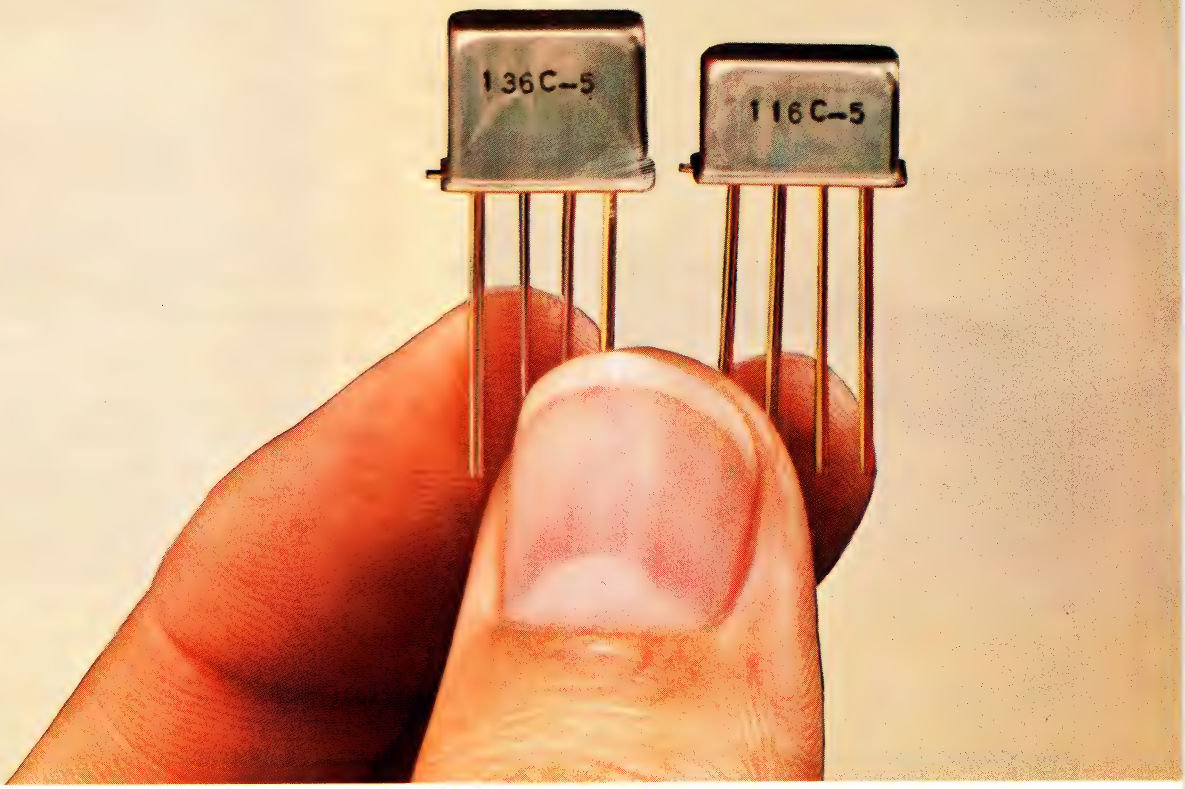
Available now from stock, the dialer is unit-priced at $2 in lots of 100.

Oki Semiconductor, 650 N. Mary Ave., Sunnyvale, Calif., 94086. Phone (408) 720-1900 [Circle 369]

Digital switch comes in fully integrated package

A digital switch is said to provide circuit switching, packet switching, time-division switching, time-division multiplexing, and advanced routing and control capabilities in one fully integrated package. The NSS switch can combine voice, data, and image transmissions on the same circuit and operates with all wide-area network

Now the world's first CMOS compatible EMR is QPL approved.



For the first time you can drive an electromechanical relay directly with the signals of most logic families—including CMOS. That means simpler board layout problems and reduced components counts for greater reliability.

The new Centigrid® relay incorporates a power FET driver in the input to amplify the signal, protects it with a large Zener diode, and packs it all together with a DPDT relay and coil suppression diode in a tiny CENTIGRID style can. And make no mistakes... it is a Centigrid relay granted QPL approval to MIL-R-28776/6 and /7. Its ruggedness and proven contact reliability are industry bywords.

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Circle 97 on reader service card

media, including terrestrial, satellite, radio, microwave, and fiber-optic facilities.

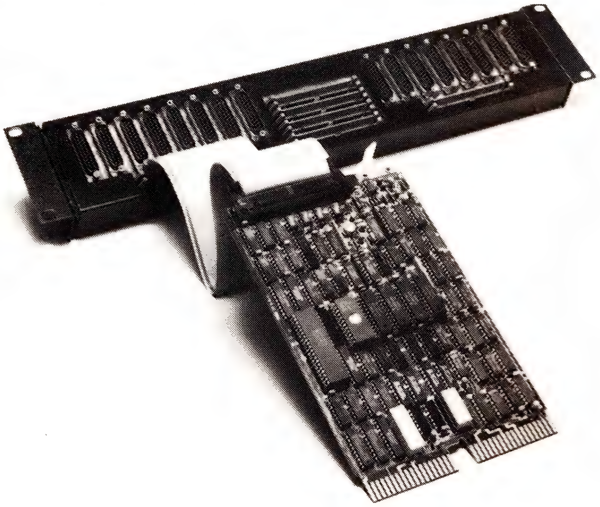
The basic unit, with an aggregate throughput of 16 Mb/s full duplex, is expandable to a system with an aggregate throughput of 64 Mb/S. The switch will handle transmission speed of 50 b/s to 1.544 Mb/s. Network management tools, redundancy, protocol support, and accounting are also included.

Evaluation units will likely be available in early 1985.

Network Switching Systems Inc., 3 Dundee Pk., Andover, Mass., 01810. Phone (617) 470-2853 [Circle 367]

Multiplexer boasts built-in verification and testing

A dual-size module, the 2134, is a DZV-compatible, eight-line asynchronous multiplexer that can replace two Digital Equipment Corp. DZV11 four-line quad-size multiplexers and is functionally equivalent to the Unibus-type DZ11. It has built-in diagnostic capabilities for terminal testing and functional verification and is compatible with LSI-11 and MicroVAX computers, including models with 22-bit addressing.



Providing data-transfer rates of up to 38.4 kilobaud as well as split-baud rates, the 2134 offers strict bus-timing control for maximum throughput. The address and interrupt functions are selectable throughout the floating ranges by a dual in-line package switch.

The double-height model 2134 is available now at $800, and can be ordered separately or with a 3½-in.-high rack-mountable distribution panel and interconnection cables.

Gen/Comp Inc., 6 Algonquin Rd., Canton, Mass. 02021.
Phone (617) 828-2008 [Circle 368]

Peak-sense-and-hold circuits capture narrow 100-ns pulses

Pulses as narrow as 100 ns maximum for a 1-V pulse and a 100-pF hold capacitor, or 200 ns maximum for a 10-V pulse and a 300-pF hold capacitor, can be captured by the AH503 and AH504 peak-sense-and-hold circuits, the manufacturer claims. With a hold capacitor of 330 pF, the droop rate will be less than 1μV/s, permitting very narrow pulses to be captured and held for further processing.

Reset time is 100 ns for the AH504 and 400 ns for the AH503. Gating time is 250 ns for the AH504, 400 ns for the AH503.

These components are intended to do the work of a circuit that otherwise would have to be built by the engineer out of subcomponents, the manufacturer says. They also are claimed to offer a size advantage.

Temperature options are available within the AH-503/AH504 group of circuits. The AH503DK operates in the temperature range from 0° to 70°C, the AH503DS in the range from –55° to +125°C, and the AH504DK in the range from 0° to 70°C.

These models are in production, and small quantities of the AH503DK and AH504DK are available for delivery from stock. In quantities of 100, prices are $88.10 for the AH503DK and $127.40 for the AH504DK and the AH503DS.

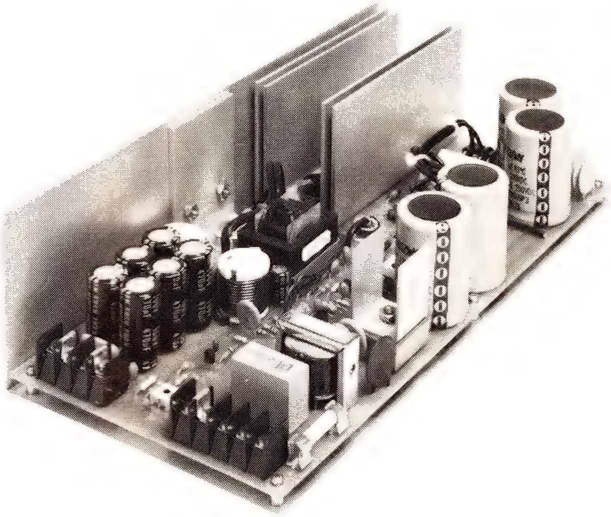
Optical Electronics Inc., P.O. Box 11140, Tucson, Ariz. 85734. Phone (602) 624-8358 [Circle 370]

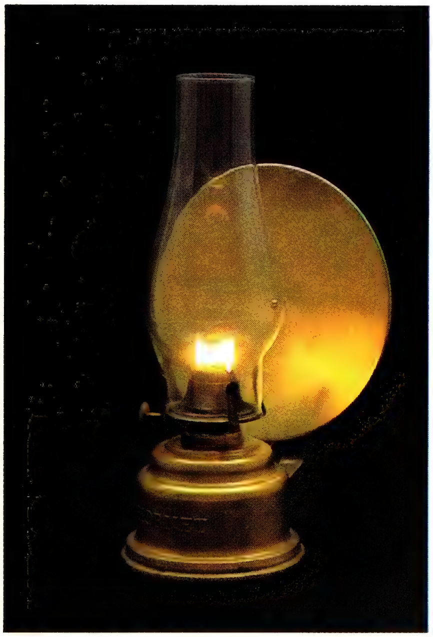
750-W single-output supplies sell for $419 apiece

Two 750-W single-output switching power supplies, designed for telecommunications applications, offer high power density, low noise output, and fast response. The SFG-24-30 provides 24 V at 30 A, and the SFG-48-15 provides 48 V at 15 A.

Both open-frame supplies measure 12 by 6 by 3¼ in. and have a power density exceeding 3.2 W/in.^{3}. They are designed to meet U.S., Canadian, and international safety standards, and their mean-time-before-failure ratings exceed 10,000 h.

Strap-selectable ac input may vary from 90 to 132 V or 180 to 240 V, 47 to 63 Hz. Soft-start circuitry, containing a distributed radio-frequency-interference filter,





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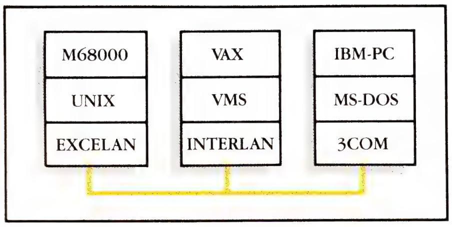

A sample network using a few of the many configurations made possible with FUSION.

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limits in-rush current at turn-on. Each power supply meets Federal Communications Commission and international RFI suppression specifications as well as the safety requirements of the Underwriters Laboratories, Canadian Standards Association, International Electrotechnical Commission 380/435, and Verband Deutscher Electrotechniker 0804/0806.

In quantities of 100, the supplies sell for $419 each, with delivery from stock.

Todd Products Corp., 50 Emjay Blvd., Brentwood, N.Y. 11717.
Phone (516) 231-3366 [Circle 373]

Predesigned supplies are custom finished

Based on 11 predesigned case sizes with power ratings from 20 to 410 W and complemented by a choice of standard user-selected electrical and mechanical options, the Flex series of power supplies should simplify the development of customized power supplies. The series also allows the user to specify his exact output rating and option requirement at lower cost and shorter development time, the company claims.

Each case size uses Verband Deutscher Electrotechniker-approved power transistor construction, allowing compliance with safety requirements for leakage current and safety spacings.

The series also has pre-approval from Underwriters Laboratories and the Canadian Standards Association and a Technische Uberwachungs-Verein certificate for VDE and International Electrotechnical Commission specifications.

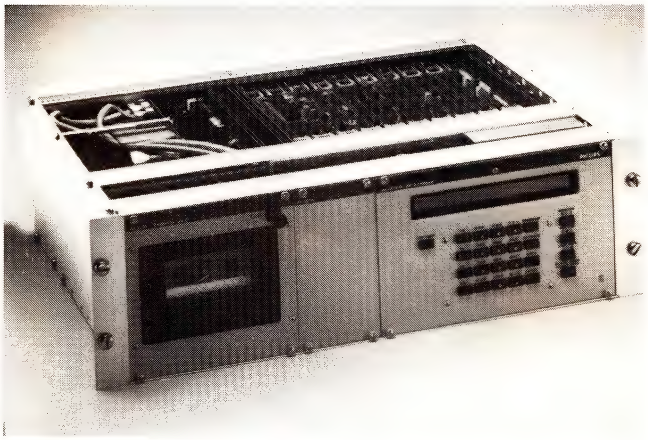
Standardized design concepts, components usage, and manufacturing processes are said to provide lower cost per watt than other designs. Quantity prices range from $30 for the 20-W FS01 package to $250 for the 410-W FS11 package.

Power-One Inc., Power One Dr., Camarillo, Calif. 93010.
Phone (805) 987-3891 [Circle 374]

Industrial data logger suits acquisition, monitoring

The Philips-type PR 2011 industrial data logger is a compact data-acquisition and monitoring system used for such industrial applications as supervision of rotating machinery, test monitoring, energy management, vehicle testing, and quality control of components. It allows the execution of complex tasks without special training and makes multichannel recording as simple as with line and multipoint recorders, the firm says.

In its basic configuration, the PR 2011 can accept up to 64 analog and up to 128 digital inputs. Up to three more frames can be added to bring the capacity up to 256 signal inputs. A built-in cassette drive is provided for parameter program loading and mobile data storage. The system can automatically convert large quantities of process values into decision-relevant information. Reliability is enhanced by the system's fully self-monitoring facilities with automatic fault location. Up to six alarm thresholds can be set on each measuring channel, and values are displayed automatically for any measuring point at which an alarm value is recorded.



The PR 2011 has a facility for remote operation and parameter setting from a video display unit that gives on-screen guidance. A serial interface allows long-distance communication between the instrument and sensors by way of serial or telephone lines.

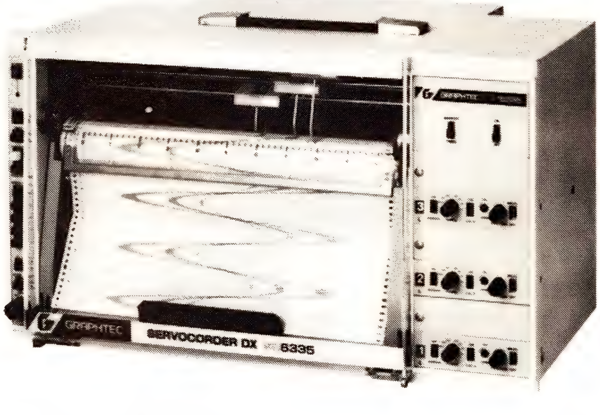
The 19-in. modular system sells for between $8,000 and $10,000 plus the cost of software. Deliveries take up to 10 weeks.

The Pyrometer Instrument Co., Northvale, N.J. 07647.
Phone (201) 768-2000 [Circle 375]

Strip-chart recorder comes in one to three channels

Intended for recording requirements in medical, laboratory, process control, and other such applications, the heavy-duty model SR 6335 is a strip-chart recorder available with one, two, or three channels.

A pen-offset compensator that eliminates time delay between channels is a standard feature on the two- and three-channel models, eliminating the manual calculation for time lag. To increase the SR 6335's versatility, 18 types of pre-amplifiers are offered. The unit also includes 20 different selectable chart speeds, as well as a chart rewind for easy review.



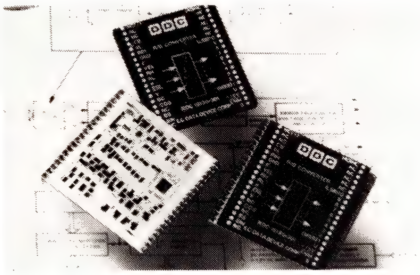
The one-channel model features a pretrigger function that automatically changes the chart speed from hour to minute at a predetermined signal level. Both signals—the one below pretrigger and the one following it—become automatically digitized and stored in memory. Eight different color pens are available.

Prices of the SR 6335, available from stock, range from $1,250 to $1,950.

Western Graphtec Inc., Advertising and Promotion Department, 12 Chrysler St., Irvine, Calif. 92718. Phone (800) 854-8385 (in Calif. (714) 770-6010) [Circle 376]

Converters eliminate need for electromechanical tachs

The RDC-19190 series of hybrid resolver-to-digital converters, according to the manufacturer, can provide linearity to within 1% of velocity output and eliminates the need for electromechanical tachometers in control systems while increasing reliability. The 2-in.^{3} Tach Eliminator can perform digital conversions and provides control systems with velocity feedback. Converters are available in 10-, 12-, 14-, and 16-bit resolution with accuracies to ±21, ±8.5, ±2.6, and ±1.3 min., respectively.



The four input-frequency ranges are from 360 Hz to 22 kHz, 600 Hz to 22 kHz, 1 kHz to 3.5 kHz, and 360 Hz to 3.5 kHz. All units operate with a reference voltage range of 4 to 50 V. The maximum tracking rates range from 400 to 6.3 revolutions/s for the 10- to 16-bit converters, respectively. The converters are primarily designed and packaged for uses in which both resolver and digital conversion and a linear velocity signal are required.

Typical applications are in motor and position control systems for ro-

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Previously, the upper shell of Model SSC 45 was painted gold to distinguish it from other models. This not only cost more but resulted in too many rejects. Oster wanted to eliminate this production step but still maintain the ADJUSTA-GROOM clipper's distinct appearance. "The quality look and feel as well as the strength, stability and economy of Plenco 04548 with its distinctive mottled color made it a good choice. We achieved a substantial reduction in production costs," Oster engineers stated.

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Circle 101 on reader service card

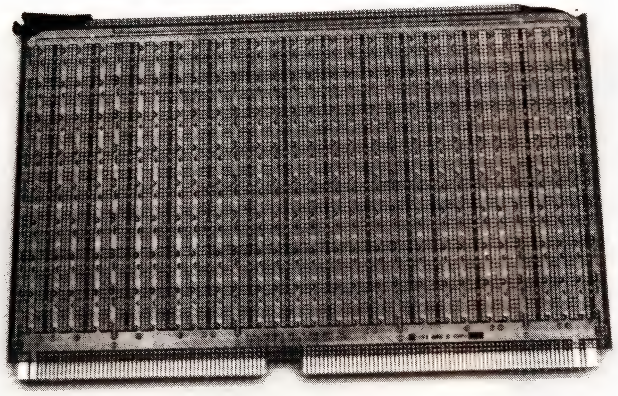
botics, computerized numerical-control-machine tooling, and precise antenna positioning. The RDC-19190 series requires 0.3 W and operates over the temperature range from 0° to 70°C. Prices start at $133 with delivery from four to eight weeks.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, N.Y., 11716. Phone (516) 567-5600 [Circle 366]

Wire-wrappable boards hold 252 14-pin DIPs

The series 4-68000B-VHF wire-wrappable socket board is a high-density version of the series 4-68000 board and holds 252 14-pin, dual in-line packages, or 22% more than its predecessor. The boards are compatible with the Motorola Versabus in form-factor and connector configuration, and will plug into any Versabus-compatible backplane and card frame.

Mechanical features include pairs of plated through-holes for individual device bypassing and committed power ground-plane bypassing. For high-frequency logic or analog applications up to 500 MHz, using the company's washer and jumper accessories produces very low inductance bypassing.



With dimensions of 14.4 by 9.25 in., the series 4-68000B-VHF boards are 0.062-in. epoxy fiberglass, 2-oz tin-plated copper, and reflowed. They come fully populated with socket pins or can be custom-pinned.

Four models are available, with 2- or 3-level pins, tin or gold bodies, and gold contacts. Models with tin bodies and 2- or 3-level pins sell for $609. Gold versions with 2- or 3-level pins cost $658. Delivery takes up to four weeks.

Hybricon Corp., Inside Sales, 410 Great Rd., Littleton, Mass. 01460. Phone (619) 486-3174 [Circle 361]

Thyristor circuits provide balanced firing signals

A line of thyristor firing circuits with isolated gate drives for safety uses digital techniques for balanced firing. The firing signals are independent of phase rotation. Eliminating the need for synchronizing transformers, the circuits' output is nearly linear to permit the use of linear analysis.

Available in single and three-phase configurations, the thyristor circuits provide firing for conduction in both positive and negative halves of the ac supply for two-quadrant operation and regenerative discharge of inductive loads. They provide hard firing signals, and operate with any 50- or 60-Hz standard line voltage up to 600 V.

List prices of the circuits, available now, begin at $267.

Reflex Inc., 303 Allens Ave., P.O. Box 1515, Providence, R.I. 02901. Phone (401) 941-4444 [Circle 362]

Heat sinks mount on DIPs without gluing

A series of heat sinks designed to slide on 8-pin dual in-line packages are said to eliminate the need for gluing and improve heat dissipation. Slide-On heat sinks have two conduction paths, one on the top and one on the bottom. Each of these surfaces has its own spring action that brings it into parallel with the DIP surfaces, resulting in maximum thermal contact regardless of DIP thickness.

Staggered fins, slotted to minimize the boundary layer effect, help provide more effective air flow. Under natural convection, with an input of 1 W, the Slide-On heat sink cools the DIP by 12°C.

A locking tab on the heat sink prevents the DIP from becoming dislodged. It also requires little maintenance and no additional board space. The Slide-On heat sink is price at 15.2¢ per 1,000. Free samples are now available.

Aavid Engineering Inc., 30 Cook Ct., Laconia, N.H. 03247. Phone (603) 524-4443 [Circle 365]

Connector carries resistor to simplify mounting LEDs

The Conxrite solderless connector provides a simplified method of electrically connecting a panel-mounted light-emitting diode. Its molded plastic body has a self-contained interchangeable ¼-W resistor, eliminating the need for an external resistor.

The connector, with its incorporated ballast resistor, can be used on circuits from 3 to 28 V with wiper-type contacts compensating for varying sizes of LED leads. It also supports and relieves stress on the LED leads providing the stability needed to eliminate broken or damaged lead problems, the company claims. Such problems as panel backout, typical of the clip and ring mount, are resolved, resulting in a more secure assembly.

Conxrite, which is part of the CNX 310 series, enables the preassembly of wiring harnesses, precluding the need for hard wiring directly to the LEDs. Thus it is easy to replace defective LEDs in final assembly, test, and field-service operations.

Available now, Conxrite is priced at 34¢ each in quantities of 10,000.

Visual Communications Co., P.O. Box 986, El Segundo, Calif. 90245. Phone (213) 822-4727 [Circle 364]

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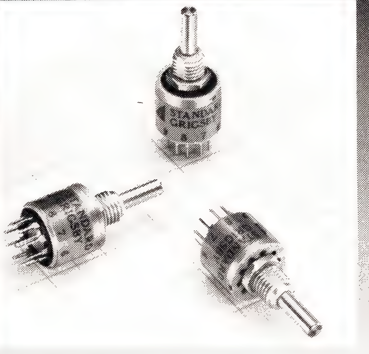

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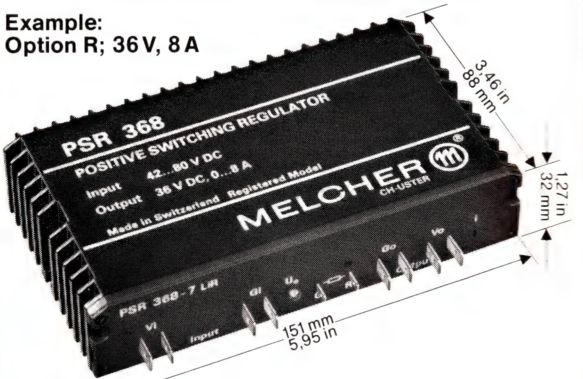

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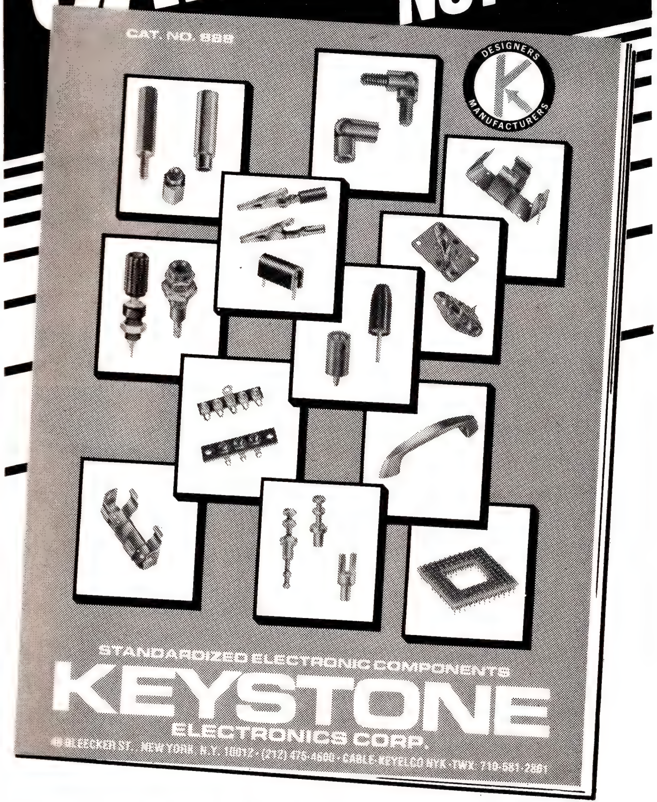
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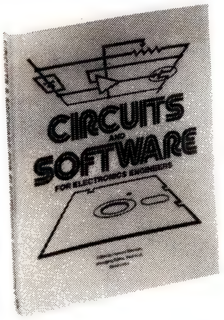

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Meetings

Videotex '84, Online Conferences Ltd. (Online Conferences Ltd., Pinner Green House, Ash Hill Drive, Pinner HA5 2AE, Middlesex, UK), The Rai Center, Amsterdam, Nov. 20-22.

China International Microelectronics/Computer Exhibition and Conference, Trade Fair Management Corp. (Harry C. Lepinske, American Exhibition Services International Inc., P.O. Box 66373, O'Hare International Airport, Chicago, Ill. 60666), Shanghai, Nov. 21-26.

Computer China '84—International Computer Technology Exhibition and Conference, Fujian Consultancy Centre for Science and Technology *et al.,* **Academic Conference,** China Microcomputer Applications Association (Adsale Exhibition Services, 21/F, Tung Wai Commercial Building, 109-111 Gloucester Rd., Wanchai, Hong Kong), Xiaman Special Economic Zone, People's Republic of China, Nov. 25-Dec. 1.

Cellular Communications, Online Conferences Ltd. (Online Conferences Ltd., Pinner Green House, Ash Hill Drive, Pinner HA5 2AE, Middlesex, UK), Westin Hotel Chicago, Chicago, Nov. 26-28.

Materials Research Society Fall Meeting, MRS (9800 McKnight Rd., Suite 327, Pittsburgh, Pa. 15237), Boston Marriott Hotel, Copley Place, Boston, Nov. 26-30.

Stress Analysis by Thermoelastic Techniques, Sira, British Society for Strain Measurement, and National Engineering Laboratory (Conference Unit, Sira Ltd., South Hill, Chislehurst, Kent BR7 5EH, UK), Meeting Rooms of the Zoological Society of London, London, Nov. 27-28.

Power Sources Conference, Power Sources Conference (Anne Weber, PSC, 3970 Altantic Ave., Suite 204, Long Beach, Calif. 90807), Sheraton-Boston Hotel and Hynes Auditorium, Boston, Nov. 27-29.

Electronic Displays '84, Network Events Ltd. (Network Events Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK), Kensington Exhibition Center, London, Nov. 27-29.

16th Precise Time and Time Interval Applications and Planning Meeting, U.S. Naval Observatory *et al.* (Sheila C. Faulkner, Time Service Division, U.S. Naval Observatory, Washington, D.C. 20390), NASA Goddard Space Flight Center, Greenbelt, Md., Nov. 27-29.

FinStrat '84, Association for Finishing Processes of SME (Brian Soloway, AFP/SME Public Relations Department, 1 SME Dr., Dearborn, Mich. 48129), Anaheim Convention Center, Anaheim, Calif., Nov. 27-29.

30th Conference on Magnetism and Magnetic Materials, IEEE *et al.* (Conference Steering Committee, c/o Richard M. Josephs, Code 5023, Naval Air Development Center, Warminster, Pa. 18974), Town and Country Hotel, San Diego, Nov. 27-30.

Robots West Conference and Exposition, Robotic Industries Assn. and Society of Manufacturing Engineers (Public Relations Department, SME, 1 SME Dr., Dearborn, Mich. 48121), Anaheim Convention Center and Hilton Hotel, Anaheim, Calif., Nov. 27-30.

1984 National Data Systems Forum and Exhibit, Transportation Data Coordinating Committee (1101 Seventeenth St. N.W., Washington, D.C. 20036), Baltimore Convention Center, Baltimore, Nov. 28-29.

Winter Simulation Conference, National Bureau of Standards *et al.* (Udo W. Pooch, Department of Computer Science, College of Engineering, Texas A&M University, College Station, Texas 77843), Sheraton-Dallas Hotel, Dallas, Nov. 28-30.

Unix Applications: Direction '85, Yates Ventures (4962 El Camino Real, Suite 111, Los Altos, Calif. 94022), Century Plaza Hotel, Los Angeles, Nov. 28-30.

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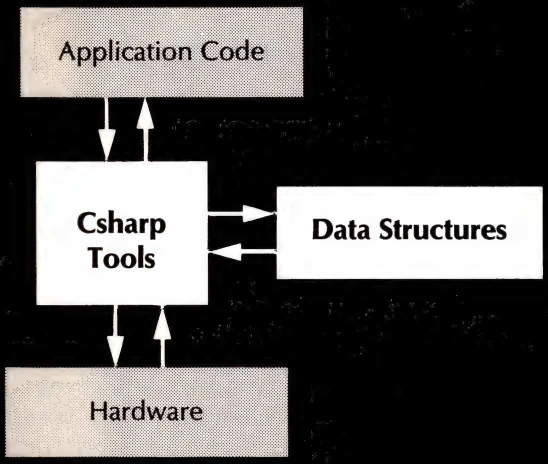

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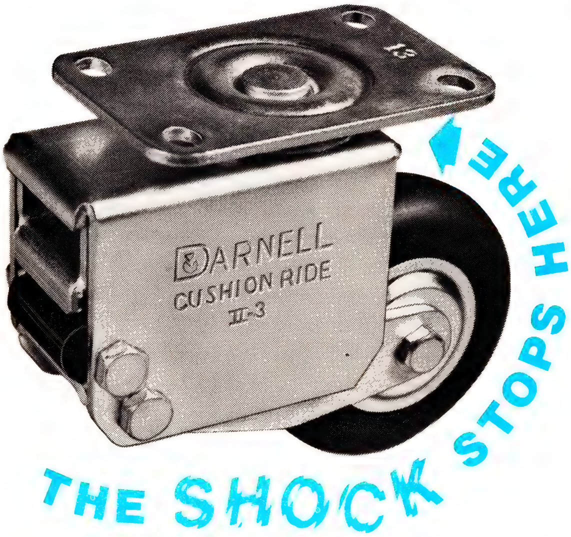

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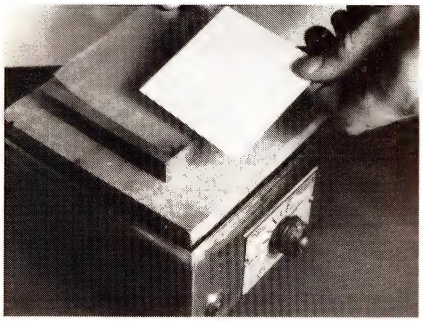


A temporary mounting adhesive, Wafer-Mount 562, is recommended for applications where a dry, preformed adhesive film is needed, as in bonding stacks of substrates for slicing. Wafer-Mount 562 melts at 195° to 210°F; after application, it readily dissolves in toluene.

Wafer-Mount 562 comes in 0.003-by-8-by-10-in. sheets, and specially sized sheets can be ordered. A standard package of 20 sheets costs $40 (larger quantities can be quoted), and delivery is from stock.

Aremco Products Inc., P.O. Box 429, Ossining, N.Y. 10562. Phone (914) 762-0685 [Circle reader service number 421]

Tubing that blocks out moisture and corrosives with an inner adhesive lining, type ST-302, has an outer wall that is flame retardant and shrinks at approximately 250°F. This combination, the manufacturer says, makes ST-302 desirable for electrical connections, wire splices, breakouts, and the repair of damaged cable jackets under harsh field conditions.

The tubing has a 2:1 shrink ratio and is available in diameters of 0.187 in. to 1.5 in. (internal diameter before shrink). Its wall thicknesses range from 0.022 in. up to 0.039 in.

Prices per 100 ft range from $91 for 0.187-in. tubing to $509.60 for 1.5-in. tubing in 5,000-ft quantities.

Cole-Flex Corp., 91 Cabot St., West Babylon, N.Y. 11704. Phone (516) 249-6150 [Circle 422]

A highly filled epoxy-based casting resin, Resin 1251, has high thermal conductivity as well as excellent insulation properties, according to the manufacturer, which recommends it for such applications as potting and encapsulating transformers, bushings, and power supplies.

Resin 1251 has a selection of four grades of hardener, ranging from general-purpose to hardeners for a variety of thermal, mechanical, and electrical applications. A low thermal coefficient of expansion and low shrinkage characteristics reduce stresses that can damage sensitive components.

Available in drums at $2.38 per lb as well as in other packaging options, Resin 1251 will be delivered in three working days.

Isochem Products Co., 99 Cook St., Lincoln, R.I. 02865. Phone (401) 723-2100 [Circle 423]

Acrylic adhesives for bonding polyimide films to rolled annealed copper foil, in flexible printed-circuit board laminates, are said by the manufacturer to have excellent adhesion, dimensional and thermal stability, and chemical resistance.

The same company also produces overlays for use with polyimide-copper or other systems, to protect foil surfaces after the circuit has been printed and etched. Produced in the form of unsupported film, the acrylic sheet adhesive is supplied semicured (B stage), 0.001 in. or 0.002 in. thick, with both surfaces covered by a release film.

Oak Materials Group Inc., 54 Church St., Hoosick Falls, N.Y. 12090. Phone (518) 686-4374 [Circle 424]

A line of laminates with thermoplastic resin cores, Tekclad targets printed-circuit-board applications requiring low electrical losses and continuous operation at high temperatures.

Bonded on both sides with electrodeposited copper foil, Tekclad laminates are compatible with direct chip-on-board attachment techniques, such as ultrasonic, thermosonic, and thermocompression bonding.

The dielectric constant is 3.13 at 100 kHz or 3.04 at 10 GHz; the dissipation factor is 0.0050 at 100 kHz, 0.0030 at 10 GHz; and the continuous operating temperature rating (UL approved) is between 140° and 180°C.

Tekclad laminates are available in three grades, and certain grades can be made transparent for see-through applications. Claddings are 1 and 2 oz (0.5 oz will be available in the fourth quarter of 1984).

Delivery is from stock to four weeks. A typical volume order ranges from $10 to $20 per ft^2 depending on weight.

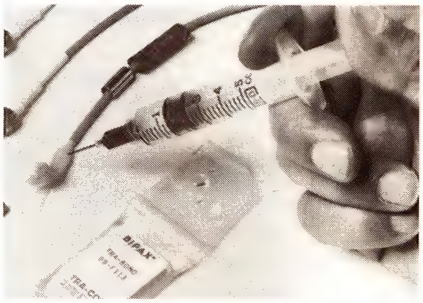
Kollmorgen Corp., 322 L.I.E. South Service Rd., Melville, N.Y. 11747. Phone (516) 454-4400 [Circle 425]

Fiber-optics components and systems and optical components can be bonded readily with an optically clear, low-viscosity epoxy adhesive, Tra-Bond F 113. The manufacturer says that it is often specified for use in fiber-optic cable terminations with pot and polish connectors.

Tra-Bond F 113 adhesive contains no solvents. The company stresses excellent wetting and wicking, and strong bonding to glass, ceramic, metal, and plastic surfaces.

The adhesive comes two-component Bipax packages. In lots of 100 packages, a 7-g kit is priced at $1.80.

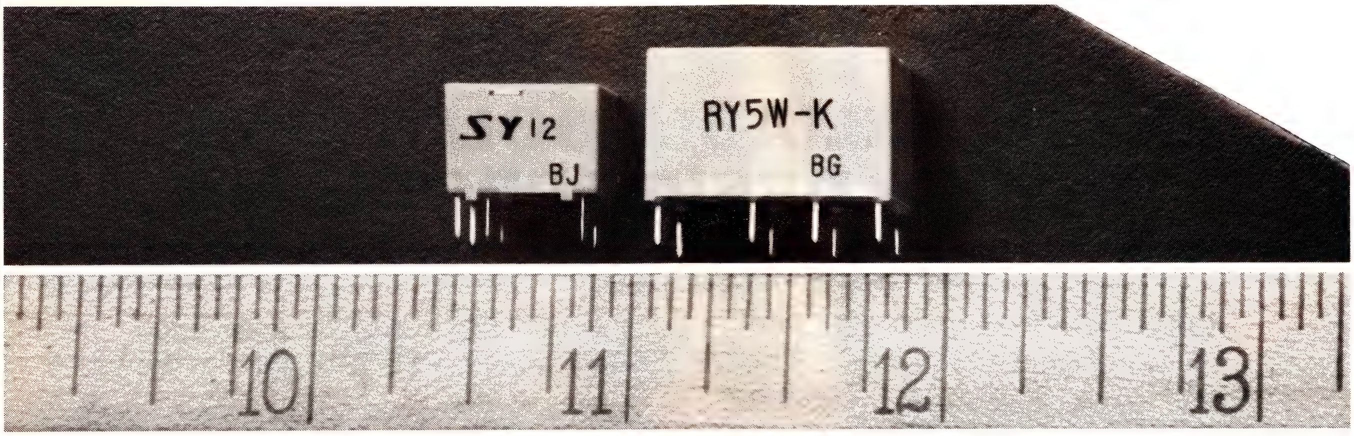
Tra-Con Inc., 55 North St., Medford, Mass. 02155. Phone (617) 391-5550 [Circle 426]



Moisture resistance and a degradation temperature above 350°C are the outstanding features of Epo-Tek 314, a two-component, 100% solids epoxy for fiber-optics assemblies. The manufacturer mentions products that may be autoclaved, chiefly medical instruments, as the principal application for this product.

With a refractive index of 1.4939, Epo-Tek 314 is recommended for optical assemblies with glass or quartz that require optical transparency. Pot life for mixed material is four days. An 8-oz trial size costs $31.

Epoxy Technology Inc., P.O. Box 567, Billerica, Mass. 01821. Phone (617) 667-3805 [Circle 427]



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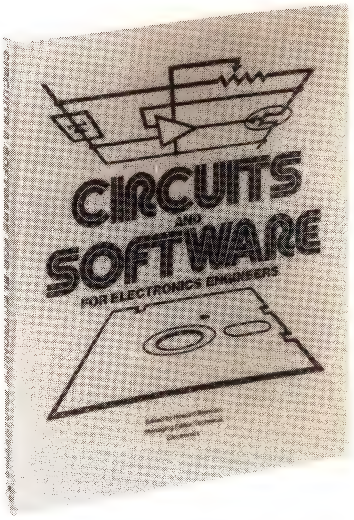

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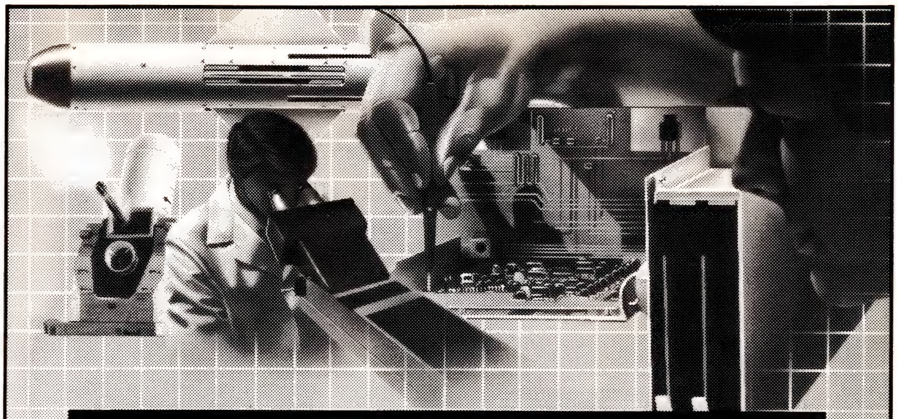

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COMPUTERS CAN'T HURT THE SMART COMPANIES

The news this week for the modern-day Luddites is not good. We all remember the original Luddites, those jolly 19th Century English workers who tried to prevent the use of labor-saving machinery by smashing it. Although their 20th Century descendants are no less devoted to the status quo, they eschew the use of sledgehammers on their mortal enemy, the computer. Instead, they rely on surveys and other up-to-date devices to call attention to their cry that the computer and its cousins will replace people and cause wholesale dislocation and unemployment, leaving only the numbing and boring tasks for the few remaining humans in the workplace.

But along comes a study from the Center for Policy Alternatives at the Massachusetts Institute of Technology. It says that, contrary to what many fear, the most profitable companies of the future will not feature mindless jobs and will not substitute computers for people in their dealings with customers. Instead, believe the experts surveyed in the study, the most competitive companies are likely to be those smart enough to use computers, robots, and the rest of the high-tech electronic family to break the assembly-line pattern of repetitive little jobs and delegate more authority to satisfy the highly skilled workforce of the future.

With computer-controlled manufacturing, "it will become more and more important for workers to understand how the entire production process fits together, rather than working with a small piece of it," concludes the study. What will become crucial as computers take over routine functions and manage robots and manufacturing functions, the study continues, is the ability and willingness of workers to solve sudden problems and to reprogram production as demands change.

The unsuccessful companies of the future, then, will be those that simply attempt to superimpose the new technologies on the old modes of rigidly hierarchical management and narrowly defined jobs. And the unsuccessful employees of the future will be those who fail to turn to their advantage the power that is afforded by computer technology.

BUYERS OF COUNTERFEITS ARE EQUALLY GUILTY

We see that two importers in Silicon Valley have been indicted on charges of smuggling counterfeit Apple Computer Inc. computers and parts, made in Taiwan, into the U.S. This is good news, considering that counterfeit computers have become a growth industry that is apt to stay that way as long it has willing manufacturers and eager customers.

Now the federal authorities have a new weapon: the copyright laws. The suspects' phony computers are loaded with Apple's copyrighted programs. This added jeopardy might make would-be criminals think twice.

We congratulate the authorities for carrying through their investigation in this case to its current stage and urge that more time be spent on such work. But as long as the dishonest customer—the one who knows where to get a IIc or Macintosh for $500—is permitted to get away with it, the problem will remain.

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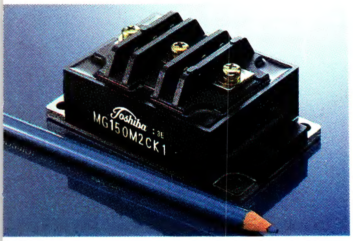

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Max. rating	ID	±15	2SK447	
		±15 × 4	MG15D4GM1	MG15G4GM1
		±15 × 6	MG15D6EM1	MG15G6EM1

TOSHIBA

Toshiba America, Inc.: Electronic Components Business Sector, Semiconductor Div.: 2441 Michelle Drive, Tustin, Calif. 92680, U.S.A. Tel. (714) 730-5000
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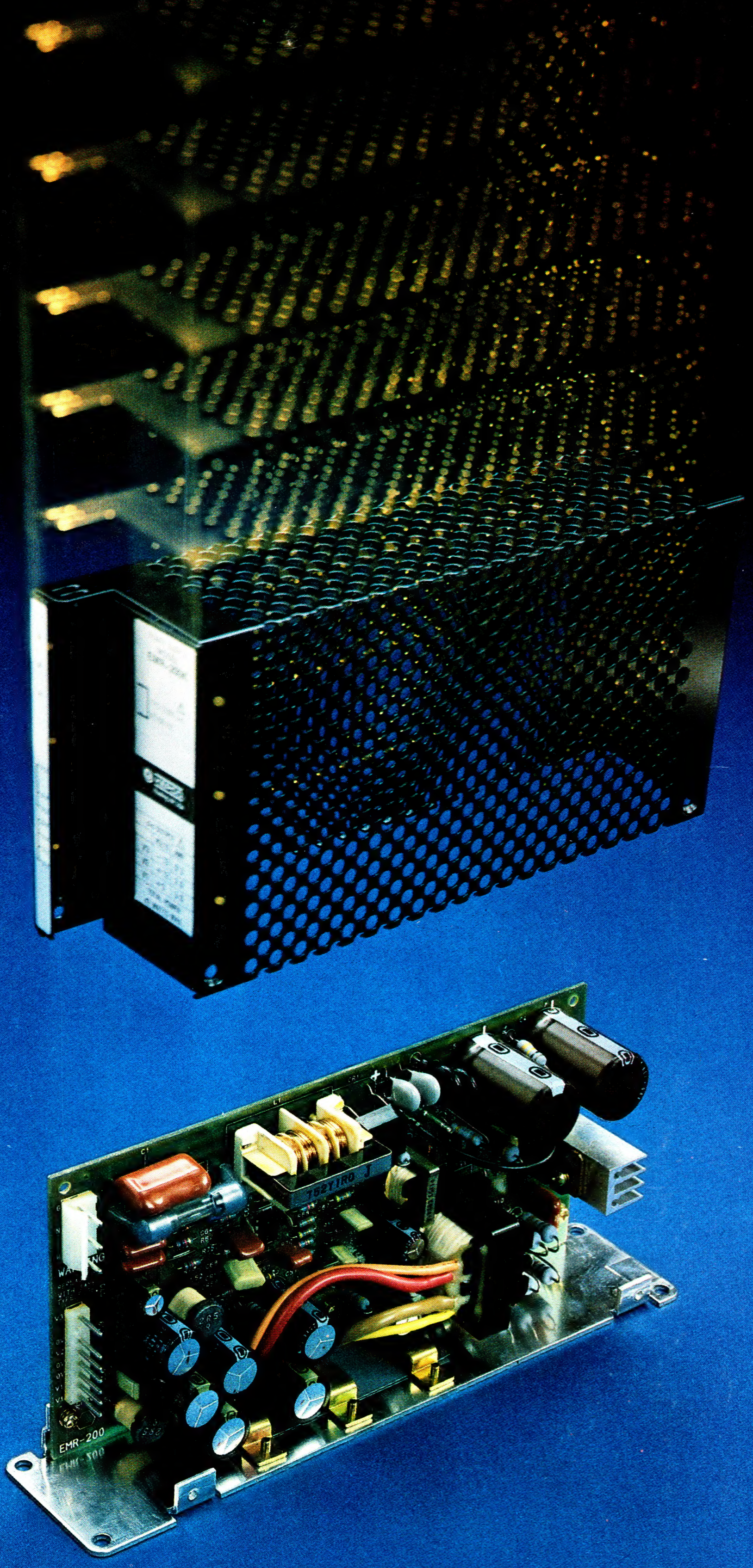
Toshiba Electronics Scandinavia AB: Banérgatan 21-23, S-115 22 Stockholm, Sweden Tel. 08-616265



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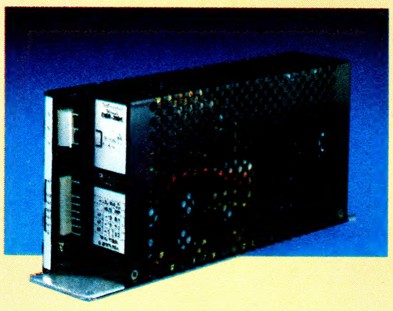
KEPCO®
POWER SUPPLIES



The first surprise is that our EMR Series of multi-output switching power supplies are fully enclosed and shielded — but are priced well below many open-frame switchers. And what makes this surprise even more surprising is the quality we've put under their perforated metal enclosures (which, incidentally, allow the EMRs to meet the radiated noise spec of VDE 0875/7.71, [level N] even when housed in a plastic-enclosed product).

One good example of this quality is the conservative design of our transformers, chokes, and on-board filters; another is their use of TDK's superior H7C1 ferrite material. As a result of these two factors, our magnetics have more ''headroom'' before saturation, and are more efficient than conventional magnetics in ordinary switchers. Still another hallmark of the quality of our EMRs is the openness and simplicity of their board layout, which is due first to computer-aided design, and second, to proprietary hybrid circuits which dramatically reduce parts population, and increase reliability while lowering cost.

The EMRs meet UL 478 and CSA C22.2-154, and their on-board EMI filters meet FCC Class B (conducted noise).

The EMRs feature money-saving pin-header input/output connectors.

There are five models, ranging from 22 to 80 Watts, with inputs as follows:

EMR Model	Output Current in Amperes			
	+5V	+12V	−12V	+24V
100K	3	0.3	0.3	—
200K	3	2	0.3	—
300K	6	1	1	—
400K	4	0.5	0.3	1
500K	5	2.3	0.3	1

Single unit prices start at $65, with substantial quantity discounts available. For a demonstration unit, write Dept. GUF-14.
KEPCO, INC., 131-38 Sanford Avenue,
Flushing, NY 11352 USA. (212) 461-7000
TWX #710 582 2631 • FAX: (212) 767-1102.

We also make open-frame switching power supplies to 150 Watts, single-output switching power supplies up to 300 Watts, and d-c to d-c converters.

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Circle 902 on reader service card